Summary Pricing					
Item	Description	Monthly Cost	NRC*	1 Year Total	3 Year Total
Item# 1	Ethernet Circuits	6,450.00	0.00	77,400.00	232,200.00
Item# 2	DS3 Circuit - Beckley to Morgantown	2,200.00	0.00	26,400.00	79,200.00
Option# 1	DS3 Circuit - Beckley to Charleston	2,200.00	0.00	26,400.00	79,200.00
Option# 2	DS3 Circuit - Charleston to Morgantown	2,200.00	0.00	26,400.00	79,200.00
	Total Cost	13,050.00	0.00	156,600.00	469,800.00

* Non-Recurring Charge (One-Time Only)

** Ethernet circuits must be segregated as defined in Exhibit C, Ethernet Segregation.

Award will be made to the Vendor with the Lowest Overall Total Cost meeting specifications.

Melissa Wright
Signature of Vendor

6-11-14
Date

Suddenlink
Company Name

108 Brent Way
Address 1

Hurricane, WV 25526
Address 2

Phone 304-760-8807

Fax 304-760-8950

Email Melissa.Wright@suddenlink.com

06/12/14 12:12:17PM
West Virginia Purchasing Division

EBA471A - Exhibit A - Pricing Pages - 3 year term

Costs must include ALL charges, including any fees, government surcharges, taxes, or any other charge associated with the service.

Location	Physical Address
Beckley	WV Public Broadcasting 124 Industrial Park Rd. Beaver, WV 25813
Charleston	WV Public Broadcasting 600 Capitol Street Charleston, WV 25301
Morgantown	WV Public Broadcasting 191 Scott Avenue Morgantown, WV 26505

Item# 1	Ethernet Circuits**	Monthly Cost	NRC*	1 Year Total	3 Year Total
1a	Beckley - 1 Gig Layer 2 Ethernet	1,750.00	0.00	21,000.00	63,000.00
1b	Beckley - 25 Meg Internet Bandwidth via LAN 10 Ethernet Port	1,200.00	0.00	14,400.00	43,200.00
1c	Charleston - 1 Gig Layer 2 Ethernet	1,750.00	0.00	21,000.00	63,000.00
1d	Morgantown - 1 Gig Layer 2 Ethernet	1,750.00	0.00	21,000.00	63,000.00
	Total Cost Item#1, Ethernet Circuits	6,450.00	0.00	77,400.00	232,200.00

Item# 2	DS3 Circuit - Beckley to Morgantown	Monthly Cost	NRC*	1 Year Total	3 Year Total
2	DS3 between Beckley and Morgantown	2,200.00	0.00	26,400.00	79,200.00
	Total Cost Item#2, DS3 Circuit - Beckley to Morgantown	2,200.00	0.00	26,400.00	79,200.00

DS3 Circuit Options

Price for these options must reflect that they will be bundled with items 1 & 2.

Option# 1	DS3 Circuit - Beckley to Charleston	Monthly Cost	NRC*	1 Year Total	3 Year Total
1	DS3 between Beckley and Charleston	2,200.00	0.00	26,400.00	79,200.00
	Total Cost Option# 1	2,200.00	0.00	26,400.00	79,200.00
Option# 2	**DS3 Circuit - Charleston to Morgantown**	**Monthly Cost**	**NRC***	**1 Year Total**	**3 Year Total**
2	DS3 between Charleston and Morgantown	2,200.00	0.00	26,400.00	79,200.00
	Total Cost Option #2	2,200.00	0.00	26,400.00	79,200.00

State of West Virginia
Department of Administration
Purchasing Division
2019 Washington Street East
Post Office Box 50130
Charleston, WV 25305-0130

Solicitation

NUMBER	PAGE
EBA471A	1

ADDRESS CORRESPONDENCE TO ATTENTION OF:
EVELYN MELTON
304-558-7023

VENDOR
RFQ COPY
TYPE NAME/ADDRESS HERE

SHIP TO
EDUCATIONAL BROADCASTING AUTHORITY
600 CAPITOL STREET
CHARLESTON, WV
25301-1223 304-558-3400

DATE PRINTED: 04/30/2014
BID OPENING DATE: 06/12/2014 BID OPENING TIME 1:30PM

LINE	QUANTITY	UOP	CAT. NO.	ITEM NUMBER	UNIT PRICE	AMOUNT

THE WEST VIRGINIA PURCHASING DIVISION IS SOLICITING BIDS ON BEHALF OF THE WEST VIRGINIA EDUCATIONAL BROADCASTING AUTHORITY (EBA) TO ESTABLISH A CONTRACT TO PROVIDE A SITE-TO-SITE CONNECTIVITY BETWEEN THREE PROPERTIES OR THE EBA AND TWO WEST VIRGINIA NETWORK (WVNET) LOCATIONS, AS WELL AS INTERNET ACCESS PER THE ATTACHED SPECIFICATIONS AND INSTRUCTIONS TO BIDDERS.

0001	3	YR	205-43	SITE-TO-SITE AND INTERNET CONNECTIVITY		

****** THIS IS THE END OF RFQ EBA471A ****** TOTAL: $469,800.00

SIGNATURE: Melissa West
TELEPHONE: 304-760-8807
DATE: 6-11-14
TITLE: Account Executive
FEIN:
ADDRESS CHANGES TO BE NOTED ABOVE

WHEN RESPONDING TO SOLICITATION, INSERT NAME AND ADDRESS IN SPACE ABOVE LABELED 'VENDOR'

Suddenlink Communications

RFP #EBA471A Responses

June 10, 2014

Suddenlink complies with terms and conditions of the bid, with the following notations, caveats, and exceptions :

3.2 Subcontracting

Suddenlink will own all fiber, and equipment with the exception of Type II circuits proposed from CityNet. The only circuits that CityNet will own are the circuits being delivered to 191 Scott Ave. and WVNet in Morgantown, WV. CityNet will own all fiber and equipment provided by their firm, acting as a subcontractor for Suddenlink.

3.4.1.5 Layer 2 Ethernet

Suddenlink will not strip away any QoS tags placed on the packets by the customer. However Suddenlink will not do QoS for the customer as we do not give any single customers traffic priority over other customer's traffic.

3.4.2.6 Digital Signal 3 (DS3) Circuit

Suddenlink has various diverse fibers paths within its core network. However there are instances within our network where these fibers may land onto a single device. There is also the possibility that if there is a fire, etc. that the Suddenlink hub site may be inoperable until the connectivity is restored.

3.5.1.1 Monitoring

Suddenlink will provide requested statistics upon request to WV EBA.

3.5.6 Mean Time to Repair

See Suddenlink Service Level Agreement included with this bid response. Suddenlink pledges four-hour response time.

3.5.8.1 Service Level Credits

See Suddenlink Service Level Agreement.

3.5.8.2 Service Level Credits

See Suddenlink Service Level Agreement

3.5.8.3 Service Level Credits

Suddenlink and Citynet both agree to the latency and packet loss commitments. If for some reason these commitments are broken it will be a management decision on how to issue credits.

3.5.8.4 Service Level Credits

See Suddenlink Service Level Agreement

Exhibit B – Connectivity

Suddenlink can provide multiple VLANS, as requested in the bid, or Suddenlink can provide a single handoff per site allowing WV EBA to use QNQ to establish and maintain their own VLANs.

Service Level Agreement

I. Scope. This Service Level Agreement ("SLA") is incorporated into the Commercial Service Agreement by and between Suddenlink Business Services, LLC ("Suddenlink") and the undersigned Customer. Suddenlink shall endeavor to meet the performance standards and services levels set forth in this SLA with respect to the Services provided to the undersigned Customer.

A. Network Availability. The Suddenlink network shall be available for use by Customer with the Services provided under the Agreement at least 99.99% of the available time ("Network Availability"). This parameter is calculated by dividing the number of minutes that the Services are available for Customer's use by the total number of minutes in each calendar month and multiplying by 100. In calculating Network Availability, the reasons or causes set forth in Section A.3 of this SLA shall not be included in determining whether Suddenlink has met the applicable performance standard for Network Availability. For example, if the Services experience an outage for One (1) day due to a Force Majeure (flood) event, and otherwise experience no other outage or Service Interruption during the applicable month, Suddenlink will be deemed to have met the Network Availability performance standard of 99.9%.

1. Service Interruption. A Service Interruption or an outage in Services is not a Default under the Agreement, but may entitle Customer to credits as provided in this SLA. A Service Interruption is a loss of Services or a degradation of signal to the Customer that adversely affects the ability of Customer to use the Services. A Service Interruption period begins when Customer makes a Trouble Report (as defined below) to Suddenlink's Network Operations Center (NOC) under the methods and procedures set forth in Section II of this SLA and ends when Suddenlink restores the Services to Customer.

2. Service Interruption Credits for Network Availability. A Credit Allowance will be given in any month during the term of the Agreement when there is a Service Interruption that qualifies for a credit allowance. The amount of the Credit Allowance shall be as follows:

Services Interruption Length	*Credit*
Less than 2 continuous hours	None
2 hours or More	1/30 of MRC due for the applicable month for each 2 hour period and additional fraction thereof

3. Exceptions to Credit Allowance. Credit Allowances shall not be provided for Services Interruptions: (i) caused by Customer, its employees, agents or subcontractors; (ii) due to failure of power or other equipment provided by Customer or the public utility company supplying power to Customer; (iii) during any period in which Suddenlink is not allowed access to the premises of Customer to access Suddenlink equipment; (iv) due to scheduled maintenance and repair; or during the maintenance window (v) caused by or due to violations of the Suddenlink Acceptable Use Policy (data customers); (vi) caused by fiber optic cable cuts on the Customer's property which are not the fault of Suddenlink; (vii) caused by a loss of service or failure of the Customer's internal wiring or other customer equipment; or (viii) due to Force Majeure events. In no event shall Customer receive more than One (1) month's MRC as credit for Service Interruptions or outages in any thirty (30) day period regardless of the number of Service Interruptions or outages. In the event that it is discovered that the Service interruption was at no fault of the Suddenlink network, and/or Suddenlink personnel and is further proven to be as a result of an issue from the Customer's network, and/or personnel a "No-Fault Trouble Call" fee will be assessed to the customer of $165 per hour with a 2-hour minimum deemed payable within the next billing cycle.

4. Major Outage. If three (3) times during the term of the Agreement, the Services to the Customer experience a Network Availability outage that falls below the 99.99% agreement, other than as a result of the causes set forth in Section A.3 above, Customer may terminate this Agreement without charge or payment of any termination charges otherwise provided in the Agreement; provided Customer complies with the notification process described in this Section 4. Within thirty (30) days of the occurrence of the 3rd Major Outage Customer shall notify Suddenlink in writing of its election to terminate this Agreement and this Agreement shall terminate upon Suddenlink's receipt of such notice. If Customer fails to notify Suddenlink within thirty (30) days of the 3rd Major Outage, of its intent to terminate, then Customer shall be deemed to have waived its right to terminate this Agreement under this Section 4 until the occurrence of a subsequent Major Outage, if any. Upon termination under this Section 4, neither party shall have any further rights, obligations, or liabilities to the other party, except those accrued through the termination date, and that expressly survive termination of this Agreement.

II. Trouble Reports. Suddenlink shall maintain a twenty-four (24) hour, seven (7) day a week point-of-contact for Customers to report Service troubles, outages or Service

Interruptions. Customer shall call Trouble Reports to **866-232-5455.** A "Trouble Report" means any report made by Customer relating to the Services or the equipment provided by Suddenlink. In the event Suddenlink receives a Trouble Report from Customer, Suddenlink shall respond within 4 hours.

III. Service Installation Intervals.

A. Service Installation and Availability. Suddenlink shall endeavor to install, provision and make the Services available for Customer's use within ten (10) business days of the Requested Service Date set forth in the Customer Service Agreement. Service availability shall mean that Suddenlink has completed its obligations to install the Suddenlink equipment and facilities set forth in the Agreement necessary to provide Customer the Services.

1. Installation Credit. Suddenlink shall provide Customer with an Installation Delay Credit if the Services are not available for Customer's use within Ten (10) business days of the Requested Service Date. In this event, Customer will be entitled to an Installation Credit of an amount equal to one month's recurring charges (MRC) for the affected Services.

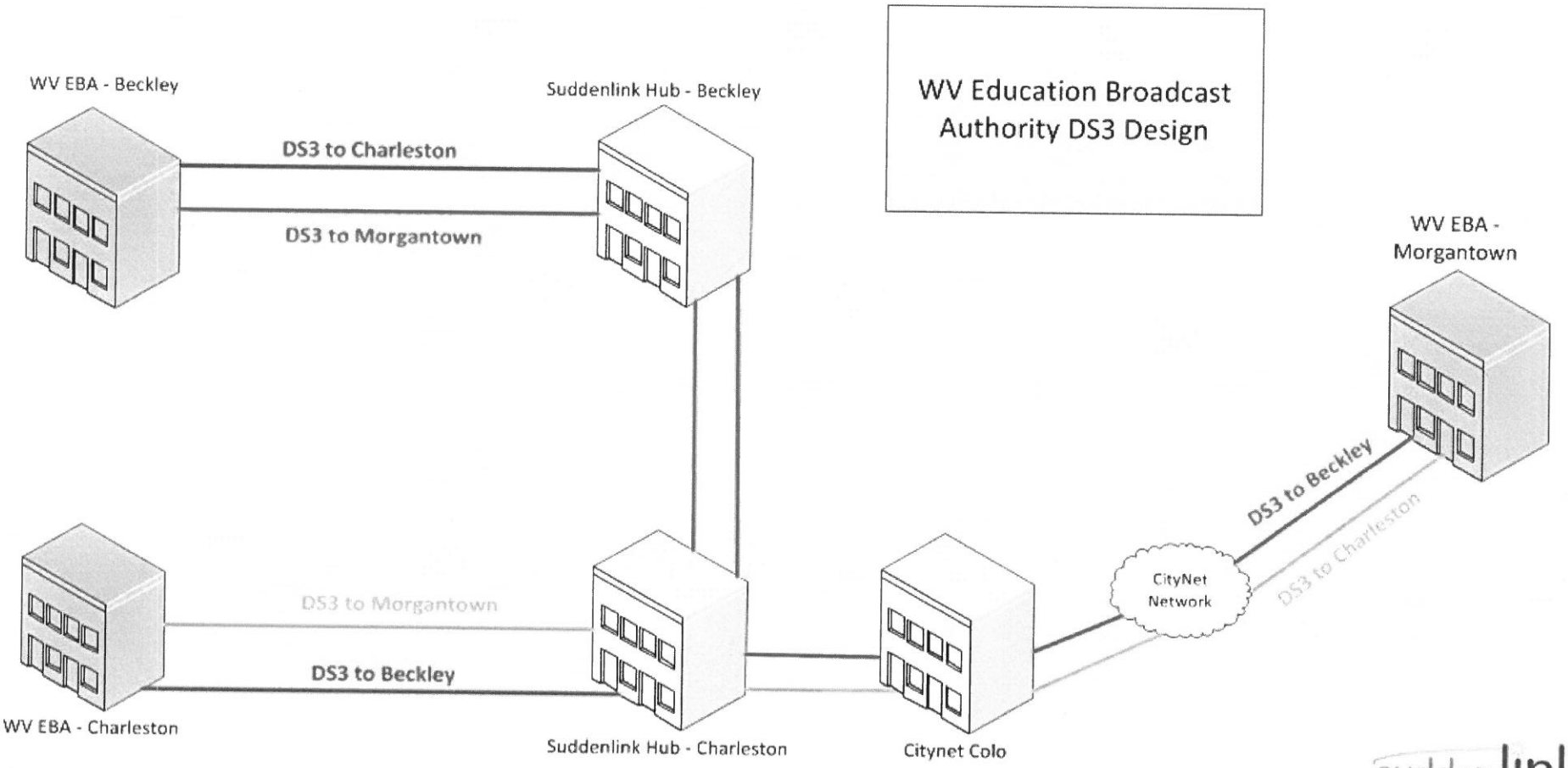
2. Exceptions to Installation Delay Credits.
Installation Delay Credits shall not be provided for Installation Delays (i) caused by or requested by Customer, its employees, agents or subcontractors; (ii) due to inability of Suddenlink to access Customer's premises due to restrictions by Customer's landlord or property owner; (iii) due to the public utility company restricting Suddenlink's access to necessary conduits or wiring in Customer's building or property; or (iv) due to Force Majeure events.

Installation Delay Credits do not apply to Suddenlink Business Phone services.

By signing below, Customer and Suddenlink agree to the terms and conditions of this Service Level Agreement.

Customer: _____
Signature: _____
Title: _____
Date: _____

Suddenlink: _____
Signature: _____
Title: _____
Date: _____


WV Education Broadcast Authority DS3 Design
WV EBA - Beckley
Suddenlink Hub - Beckley
DS3 to Charleston
DS3 to Morgantown
WV EBA - Morgantown
DS3 to Beckley
DS3 to Charleston
CityNet Network
DS3 to Morgantown
DS3 to Beckley
WV EBA - Charleston
Suddenlink Hub - Charleston
Citynet Colo
suddenlink

DS3 Node List

Beckley to Charleston DS3

1. WV EBA Beckley
2. Suddenlink Hub – Beckley
3. Suddenlink Hub – Charleston
4. WV EBA Charleston

Beckley to Morgantown DS3

1. WV EBA Beckley
2. Suddenlink Hub – Beckley
3. Suddenlink Hub – Charleston
4. Suddenlink/CityNet Colo
5. CityNet Network (1 Hop)
6. WV EBA Morgantown

Charleston to Morgantown DS3

1. WV EBA – Charleston
2. Suddenlink Hub – Charleston
3. Suddenlink/CityNet Colo
4. CityNet Network (1 Hop)
5. WV EBA – Morgantown

Charleston to Beckley DS3

1. WV EBA – Charleston
2. Suddenlink Hub – Charleston
3. Suddenlink Hub – Beckley
4. WV EBA – Beckley

Morgantown to Beckley DS3

1. WV EBA – Morgantown
2. CityNet Network (1 Hop)
3. Suddenlink/CityNet Colo
4. Suddenlink Hub – Charleston
5. Suddenlink Hub – Beckley
6. WV EBA – Beckley

Morgantown to Charleston DS3

1. WV EBA – Morgantown
2. CityNet Network (1 Hop)
3. Suddenlink/CityNet Colo
4. Suddenlink Hub – Charleston
5. WV EBA - Charleston

CERTIFICATION AND SIGNATURE PAGE

By signing below, I certify that I have reviewed this Solicitation in its entirety; understand the requirements, terms and conditions, and other information contained herein; that I am submitting this bid or proposal for review and consideration; that I am authorized by the bidder to execute this bid or any documents related thereto on bidder's behalf; that I am authorized to bind the bidder in a contractual relationship; and that to the best of my knowledge, the bidder has properly registered with any State agency that may require registration.

Suddenlink
(Company)

Melissa Wright
(Authorized Signature)

Melissa Wright, Account Executive
(Representative Name, Title)

304-760-8807 304-760-8950
(Phone Number) (Fax Number)

6-11-14
(Date)

ADDENDUM ACKNOWLEDGEMENT FORM
SOLICITATION NO.: EBA471A

Instructions: Please acknowledge receipt of all addenda issued with this solicitation by completing this addendum acknowledgment form. Check the box next to each addendum received and sign below. Failure to acknowledge addenda may result in bid disqualification.

Acknowledgment: I hereby acknowledge receipt of the following addenda and have made the necessary revisions to my proposal, plans and/or specification, etc.

Addendum Numbers Received:
(Check the box next to each addendum received)

- [x] Addendum No. 1
- [x] Addendum No. 2
- [ ] Addendum No. 3
- [ ] Addendum No. 4
- [ ] Addendum No. 5
- [ ] Addendum No. 6
- [ ] Addendum No. 7
- [ ] Addendum No. 8
- [ ] Addendum No. 9
- [ ] Addendum No. 10

I understand that failure to confirm the receipt of addenda may be cause for rejection of this bid. I further understand that any verbal representation made or assumed to be made during any oral discussion held between Vendor's representatives and any state personnel is not binding. Only the information issued in writing and added to the specifications by an official addendum is binding.

Suddenlink
Company

Authorized Signature

6-11-14
Date

NOTE: This addendum acknowledgement should be submitted with the bid to expedite document processing.

11 MISCELLANEOUS:

11.1 Contract Manager: During its performance of this Contract, Vendor must designate and maintain a primary contract manager responsible for overseeing Vendor's responsibilities under this Contract. The Contract manager must be available during normal business hours to address any customer service or other issues related to this Contract. Vendor should list its Contract manager and his or her contact information below.

Contract Manager: Brad Estep
Telephone Number: 304-760-8928
Fax Number: 304-760-8950
Email Address: Brad.Estep@suddenlink.com

Rev. 04/14

State of West Virginia

VENDOR PREFERENCE CERTIFICATE

Certification and application* is hereby made for Preference in accordance with ***West Virginia Code***, §5A-3-37. (Does not apply to construction contracts). ***West Virginia Code***, §5A-3-37, provides an opportunity for qualifying vendors to request (at the time of bid) preference for their residency status. Such preference is an evaluation method only and will be applied only to the cost bid in accordance with the ***West Virginia Code***. This certificate for application is to be used to request such preference. The Purchasing Division will make the determination of the Vendor Preference, if applicable.

1. **Application is made for 2.5% vendor preference for the reason checked:**
   ____ Bidder is an individual resident vendor and has resided continuously in West Virginia for four (4) years immediately preceding the date of this certification; **or,**
   ____ Bidder is a partnership, association or corporation resident vendor and has maintained its headquarters or principal place of business continuously in West Virginia for four (4) years immediately preceding the date of this certification; or 80% of the ownership interest of Bidder is held by another individual, partnership, association or corporation resident vendor who has maintained its headquarters or principal place of business continuously in West Virginia for four (4) years immediately preceding the date of this certification; **or,**
   ____ Bidder is a nonresident vendor which has an affiliate or subsidiary which employs a minimum of one hundred state residents and which has maintained its headquarters or principal place of business within West Virginia continuously for the four (4) years immediately preceding the date of this certification; **or,**

2. **Application is made for 2.5% vendor preference for the reason checked:**
   ____ Bidder is a resident vendor who certifies that, during the life of the contract, on average at least 75% of the employees working on the project being bid are residents of West Virginia who have resided in the state continuously for the two years immediately preceding submission of this bid; **or,**

3. **Application is made for 2.5% vendor preference for the reason checked:**
   ____ Bidder is a nonresident vendor employing a minimum of one hundred state residents or is a nonresident vendor with an affiliate or subsidiary which maintains its headquarters or principal place of business within West Virginia employing a minimum of one hundred state residents who certifies that, during the life of the contract, on average at least 75% of the employees or Bidder's affiliate's or subsidiary's employees are residents of West Virginia who have resided in the state continuously for the two years immediately preceding submission of this bid; **or,**

4. **Application is made for 5% vendor preference for the reason checked:**
   ____ Bidder meets either the requirement of both subdivisions (1) and (2) or subdivision (1) and (3) as stated above; **or,**

5. **Application is made for 3.5% vendor preference who is a veteran for the reason checked:**
   ____ Bidder is an individual resident vendor who is a veteran of the United States armed forces, the reserves or the National Guard and has resided in West Virginia continuously for the four years immediately preceding the date on which the bid is submitted; **or,**

6. **Application is made for 3.5% vendor preference who is a veteran for the reason checked:**
   ____ Bidder is a resident vendor who is a veteran of the United States armed forces, the reserves or the National Guard, if, for purposes of producing or distributing the commodities or completing the project which is the subject of the vendor's bid and continuously over the entire term of the project, on average at least seventy-five percent of the vendor's employees are residents of West Virginia who have resided in the state continuously for the two immediately preceding years.

7. **Application is made for preference as a non-resident small, women- and minority-owned business, in accordance with *West Virginia Code* §5A-3-59 and *West Virginia Code of State Rules*.**
   ____ Bidder has been or expects to be approved prior to contract award by the Purchasing Division as a certified small, women- and minority-owned business.

Bidder understands if the Secretary of Revenue determines that a Bidder receiving preference has failed to continue to meet the requirements for such preference, the Secretary may order the Director of Purchasing to: (a) reject the bid; or (b) assess a penalty against such Bidder in an amount not to exceed 5% of the bid amount and that such penalty will be paid to the contracting agency or deducted from any unpaid balance on the contract or purchase order.

By submission of this certificate, Bidder agrees to disclose any reasonably requested information to the Purchasing Division and authorizes the Department of Revenue to disclose to the Director of Purchasing appropriate information verifying that Bidder has paid the required business taxes, provided that such information does not contain the amounts of taxes paid nor any other information deemed by the Tax Commissioner to be confidential.

Under penalty of law for false swearing (West Virginia Code, §61-5-3), Bidder hereby certifies that this certificate is true and accurate in all respects; and that if a contract is issued to Bidder and if anything contained within this certificate changes during the term of the contract, Bidder will notify the Purchasing Division in writing immediately.

Bidder: Suddenlink Signed: [signature]

Date: 6-11-14 Title: Regional Sales mgr.

RFQ No. EBA471A

STATE OF WEST VIRGINIA
Purchasing Division

PURCHASING AFFIDAVIT

MANDATE: Under W. Va. Code §5A-3-10a, no contract or renewal of any contract may be awarded by the state or any of its political subdivisions to any vendor or prospective vendor when the vendor or prospective vendor or a related party to the vendor or prospective vendor is a debtor and: (1) the debt owed is an amount greater than one thousand dollars in the aggregate; or (2) the debtor is in employer default.

EXCEPTION: The prohibition listed above does not apply where a vendor has contested any tax administered pursuant to chapter eleven of the W. Va. Code, workers' compensation premium, permit fee or environmental fee or assessment and the matter has not become final or where the vendor has entered into a payment plan or agreement and the vendor is not in default of any of the provisions of such plan or agreement.

DEFINITIONS:

"Debt" means any assessment, premium, penalty, fine, tax or other amount of money owed to the state or any of its political subdivisions because of a judgment, fine, permit violation, license assessment, defaulted workers' compensation premium, penalty or other assessment presently delinquent or due and required to be paid to the state or any of its political subdivisions, including any interest or additional penalties accrued thereon.

"Employer default" means having an outstanding balance or liability to the old fund or to the uninsured employers' fund or being in policy default, as defined in W. Va. Code § 23-2c-2, failure to maintain mandatory workers' compensation coverage, or failure to fully meet its obligations as a workers' compensation self-insured employer. An employer is not in employer default if it has entered into a repayment agreement with the Insurance Commissioner and remains in compliance with the obligations under the repayment agreement.

"Related party" means a party, whether an individual, corporation, partnership, association, limited liability company or any other form or business association or other entity whatsoever, related to any vendor by blood, marriage, ownership or contract through which the party has a relationship of ownership or other interest with the vendor so that the party will actually or by effect receive or control a portion of the benefit, profit or other consideration from performance of a vendor contract with the party receiving an amount that meets or exceed five percent of the total contract amount.

AFFIRMATION: By signing this form, the vendor's authorized signer affirms and acknowledges under penalty of law for false swearing (*W. Va. Code* §61-5-3) that neither vendor nor any related party owe a debt as defined above and that neither vendor nor any related party are in employer default as defined above, unless the debt or employer default is permitted under the exception above.

WITNESS THE FOLLOWING SIGNATURE:

Vendor's Name: SuddenLink

Authorized Signature: _____ Date: 6-11-14

State of West Virginia

County of Putnam, to-wit:

Taken, subscribed, and sworn to before me this 11th day of June, 2014

My Commission expires February 25, 2023

AFFIX SEAL HERE

NOTARY PUBLIC _____

OFFICIAL SEAL
Notary Public, State of West Virginia
MICHELLE CALLIHAN
3598 Balls Branch Rd.
Culloden, WV 25510
My commission expires February 25, 2023

State of West Virginia
Department of Administration
Purchasing Division
2019 Washington Street East
Post Office Box 50130
Charleston, WV 25305-0130

Solicitation

NUMBER	PAGE
EBA471A	1

ADDRESS CORRESPONDENCE TO ATTENTION OF:
EVELYN MELTON
304-558-7023

VENDOR
RFQ COPY
TYPE NAME/ADDRESS HERE

SHIP TO
EDUCATIONAL BROADCASTING
AUTHORITY
600 CAPITOL STREET

CHARLESTON, WV
25301-1223 304-558-3400

DATE PRINTED: 05/29/2014

BID OPENING DATE: 06/12/2014 BID OPENING TIME 1:30PM

LINE	QUANTITY	UOP	CAT NO	ITEM NUMBER	UNIT PRICE	AMOUNT
				ADDENDUM NO. 2		
				ADDENDUM ISSUED;		
				1. TO PROVIDE RESPONSES TO VENDORS' QUESTIONS REGARDING THE ABOVE SOLICITATION.		
				2. TO PROVIDE ADDENDUM ACKNOWLEDGMENT. THIS DOCUMENT SHOULD BE SIGNED AND RETURNED WITH YOUR BID. FAILURE TO SIGN AND RETURN MAY RESULT IN THE DISQUALIFICATION OF YOUR BID.		
				END OF ADDENDUM NO. 2		
0001	3	YR	205-43	SITE-TO-SITE AND INTERNET CONNECTIVITY		
				****** THIS IS THE END OF RFQ EBA471A ****** TOTAL:		

SIGNATURE: Melissa Wolt
TELEPHONE: 304-760-8807
DATE: 6-11-14
TITLE: Account Executive
FEIN:
ADDRESS CHANGES TO BE NOTED ABOVE

WHEN RESPONDING TO SOLICITATION, INSERT NAME AND ADDRESS IN SPACE ABOVE LABELED 'VENDOR'

SOLICITATION NUMBER: EBA471A
Addendum Number: 2

The purpose of this addendum is to modify the solicitation identified as ("Solicitation") to reflect the change(s) identified and described below.

Applicable Addendum Category:

| | Modify bid opening date and time

| | Modify specifications of product or service being sought

|✓| Attachment of vendor questions and responses

| | Attachment of pre-bid sign-in sheet

| | Correction of error

|✓| Other

Description of Modification to Solicitation:

1. To provide responses to questions received.
2. To provide Addendum Acknowledgment.

Additional Documentation: Documentation related to this Addendum (if any) has been included herewith as Attachment A and is specifically incorporated herein by reference.

Terms and Conditions:

1. All provisions of the Solicitation and other addenda not modified herein shall remain in full force and effect.

2. Vendor should acknowledge receipt of all addenda issued for this Solicitation by completing an Addendum Acknowledgment, a copy of which is included herewith. Failure to acknowledge addenda may result in bid disqualification. The addendum acknowledgement should be submitted with the bid to expedite document processing.

ATTACHMENT A

WVPBS RFQ EBA471A List of Questions

Question 1) Exhibit B Connectivity: Please explain why the diagram has (25Meg Reserve) listed. The circuits in Exhibit C show 50Meg. Should these circuits perform at 50Mb?

Answer 1) These circuits should perform at 50 Mb. In Beckley we will have 25 Meg vendor provided Internet and wish a reserve to expand the Beckley Internet bandwidth. In Charleston and Morgantown we will be carrying both WVNet Internet traffic and other traffic to the State network. If the vendor provides 50 Mb connectivity (as diagrammed) we will work with WVNet on their connections. If there are issues provisioning this leg of the circuit as diagrammed, we will work with the winning vendor to resolve them.

Question 2) Exhibit C: Example mentions LAN 1 ports communicating from Beckley to Morgantown and Charleston however LAN 1 segregation in the above chart only shows LAN #1 appearing in Beckley and Charleston. Is this is a typo?

Answer 2) Yes, this is a typo. LAN #4 would be an accurate example.

Question 3) Lumos requests a new copy of Beckley Floor Plans this document was changed at the Pre-Bid meeting.

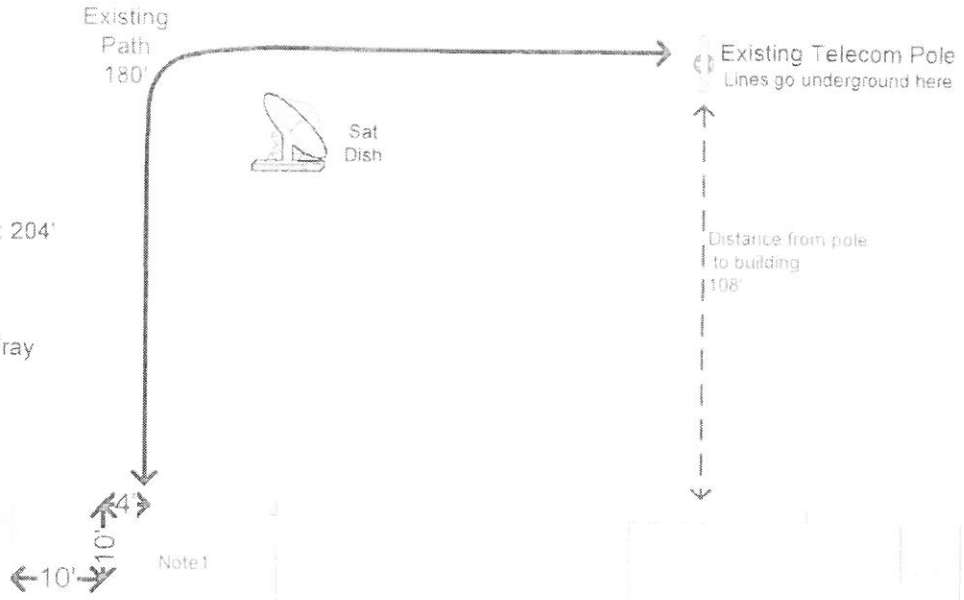
Answer 3) Attached.

WSWP-TV
124 Industrial Pk Rd
Beaver, WV 25813

Approximate Total Length DS3: 204'

Cable Tray is 9'3" from floor

Note 1: Interior run is in Cable Tray



ADDENDUM ACKNOWLEDGEMENT FORM
SOLICITATION NO.: EBA471A

Instructions: Please acknowledge receipt of all addenda issued with this solicitation by completing this addendum acknowledgment form. Check the box next to each addendum received and sign below. Failure to acknowledge addenda may result in bid disqualification.

Acknowledgment: I hereby acknowledge receipt of the following addenda and have made the necessary revisions to my proposal, plans and/or specification, etc.

Addendum Numbers Received:
(Check the box next to each addendum received)

[ ]	Addendum No. 1	[ ]	Addendum No. 6
[X]	Addendum No. 2	[ ]	Addendum No. 7
[ ]	Addendum No. 3	[ ]	Addendum No. 8
[ ]	Addendum No. 4	[ ]	Addendum No. 9
[ ]	Addendum No. 5	[ ]	Addendum No. 10

I understand that failure to confirm the receipt of addenda may be cause for rejection of this bid. I further understand that any verbal representation made or assumed to be made during any oral discussion held between Vendor's representatives and any state personnel is not binding. Only the information issued in writing and added to the specifications by an official addendum is binding.

Suddenlink
Company

Melissa Wyatt
Authorized Signature

6-11-14
Date

NOTE: This addendum acknowledgement should be submitted with the bid to expedite document processing.

INSTRUCTIONS TO VENDORS SUBMITTING BIDS

1. **REVIEW DOCUMENTS THOROUGHLY:** The attached documents contain a solicitation for bids. Please read these instructions and all documents attached in their entirety. These instructions provide critical information about requirements that if overlooked could lead to disqualification of a Vendor's bid. All bids must be submitted in accordance with the provisions contained in these instructions and the Solicitation. Failure to do so may result in disqualification of Vendor's bid.

2. **MANDATORY TERMS:** The Solicitation may contain mandatory provisions identified by the use of the words "must," "will," and "shall." Failure to comply with a mandatory term in the Solicitation will result in bid disqualification.

3. **PREBID MEETING:** The item identified below shall apply to this Solicitation.

☐ A pre-bid meeting will not be held prior to bid opening.

☐ A **NON-MANDATORY PRE-BID** meeting will be held at the following place and time:

☑ A **MANDATORY PRE-BID** meeting will be held at the following place and time:

Beckley, WV Office - May 16, 2014 @ 10:30 a.m.
* 124 Industrial Park Road, Beaver, WV 25813
Morgantown, WV Office - May 19, 2014 @ 11:00 a.m.
* 191 Scott Avenue, Morgantown, WV 26505
Charleston, WV Office - MAy 20, 2014 @ 10:30 a.m.
* 600 Capitol Street, Charleston WV 25301

All Vendors submitting a bid must attend the mandatory pre-bid meeting. Failure to attend the mandatory pre-bid meeting shall result in disqualification of the Vendor's bid. No one person attending the pre-bid meeting may represent more than one Vendor.

An attendance sheet provided at the pre-bid meeting shall serve as the official document verifying attendance. The State will not accept any other form of proof or documentation to verify attendance. Any person attending the pre-bid meeting on behalf of a Vendor must list on the attendance sheet his or her name and the name of the Vendor he or she is representing. Additionally, the person attending the pre-bid meeting should include the Vendor's E-Mail address, phone number, and Fax number on the attendance sheet. It is the Vendor's responsibility to locate the attendance sheet and provide the required information. Failure to complete the attendance sheet as required may result in disqualification of Vendor's bid.

All Vendors should arrive prior to the starting time for the pre-bid. Vendors who arrive after the starting time but prior to the end of the pre-bid will be permitted to sign in, but are charged with knowing all matters discussed at the pre-bid.

Questions submitted at least five business days prior to a scheduled pre-bid will be discussed at the pre-bid meeting if possible. Any discussions or answers to questions at the pre-bid meeting are preliminary in nature and are non-binding. Official and binding answers to questions will be published in a written addendum to the Solicitation prior to bid opening.

4. **VENDOR QUESTION DEADLINE:** Vendors may submit questions relating to this Solicitation to the Purchasing Division. Questions must be submitted in writing. All questions must be submitted on or before the date listed below and to the address listed below in order to be considered. A written response will be published in a Solicitation addendum if a response is possible and appropriate. Non-written discussions, conversations, or questions and answers regarding this Solicitation are preliminary in nature and are non-binding.

Question Submission Deadline: May 23, 2014 -end of business

Submit Questions to: Evelyn P. Melton
2019 Washington Street, East
Charleston, WV 25305
Fax: (304) 558-4115
(Vendors should not use this fax number for bid submission)
Email: evelyn.p.melton@wv.gov

5. **VERBAL COMMUNICATION:** Any verbal communication between the Vendor and any State personnel is not binding, including that made at the mandatory pre-bid conference. Only information issued in writing and added to the Solicitation by an official written addendum by the Purchasing Division is binding.

6. **BID SUBMISSION:** All bids must be signed and delivered by the Vendor to the Purchasing Division at the address listed below on or before the date and time of the bid opening. Any bid received by the Purchasing Division staff is considered to be in the possession of the Purchasing Division and will not be returned for any reason. The Purchasing Division will not accept bids, modification of bids, or addendum acknowledgment forms via e-mail. Acceptable delivery methods include hand delivery, delivery by courier, or facsimile. The bid delivery address is:

Department of Administration, Purchasing Division
2019 Washington Street East
Charleston, WV 25305-0130

The bid should contain the information listed below on the face of the envelope or the bid may not be considered:

SEALED BID: _____
BUYER: _____
SOLICITATION NO.: _____
BID OPENING DATE: _____
BID OPENING TIME: _____
FAX NUMBER: _____

In the event that Vendor is responding to a request for proposal, the Vendor shall submit one original technical and one original cost proposal plus _____ convenience copies of each to the Purchasing Division at the address shown above. Additionally, the Vendor should identify the bid type as either a technical or cost proposal on the face of each bid envelope submitted in response to a request for proposal as follows:

BID TYPE: ☐ Technical
☐ Cost

7. **BID OPENING:** Bids submitted in response to this Solicitation will be opened at the location identified below on the date and time listed below. Delivery of a bid after the bid opening date and time will result in bid disqualification. For purposes of this Solicitation, a bid is considered delivered when time stamped by the official Purchasing Division time clock.

Bid Opening Date and Time: June 12, 2014 @ 1:30 P.M.

Bid Opening Location: Department of Administration, Purchasing Division
2019 Washington Street East
Charleston, WV 25305-0130

8. **ADDENDUM ACKNOWLEDGEMENT:** Changes or revisions to this Solicitation will be made by an official written addendum issued by the Purchasing Division. Vendor should acknowledge receipt of all addenda issued with this Solicitation by completing an Addendum Acknowledgment Form, a copy of which is included herewith. Failure to acknowledge addenda may result in bid disqualification. The addendum acknowledgement should be submitted with the bid to expedite document processing.

9. **BID FORMATTING:** Vendor should type or electronically enter the information onto its bid to prevent errors in the evaluation. Failure to type or electronically enter the information may result in bid disqualification.

GENERAL TERMS AND CONDITIONS:

1. **CONTRACTUAL AGREEMENT:** Issuance of a Purchase Order signed by the Purchasing Division Director, or his designee, and approved as to form by the Attorney General's office constitutes acceptance of this Contract made by and between the State of West Virginia and the Vendor. Vendor's signature on its bid signifies Vendor's agreement to be bound by and accept the terms and conditions contained in this Contract.

2. **DEFINITIONS:** As used in this Solicitation/Contract, the following terms shall have the meanings attributed to them below. Additional definitions may be found in the specifications included with this Solicitation/Contract.

   2.1 "Agency" or **"Agencies"** means the agency, board, commission, or other entity of the State of West Virginia that is identified on the first page of the Solicitation or any other public entity seeking to procure goods or services under this Contract.

   2.2 "Contract" means the binding agreement that is entered into between the State and the Vendor to provide the goods and services requested in the Solicitation.

   2.3 "Director" means the Director of the West Virginia Department of Administration, Purchasing Division.

   2.4 "Purchasing Division" means the West Virginia Department of Administration, Purchasing Division.

   2.5 "Purchase Order" means the document signed by the Agency and the Purchasing Division, and approved as to form by the Attorney General, that identifies the Vendor as the successful bidder and Contract holder.

   2.6 "Solicitation" means the official solicitation published by the Purchasing Division and identified by number on the first page thereof.

   2.7 "State" means the State of West Virginia and/or any of its agencies, commissions, boards, etc. as context requires.

   2.8 "Vendor" or **"Vendors"** means any entity submitting a bid in response to the Solicitation, the entity that has been selected as the lowest responsible bidder, or the entity that has been awarded the Contract as context requires.

3. **CONTRACT TERM; RENEWAL; EXTENSION:** The term of this Contract shall be determined in accordance with the category that has been identified as applicable to this Contract below:

☑ **Term Contract**

Initial Contract Term: This Contract becomes effective on upon award

and extends for a period of one (1) year(s).

Renewal Term: This Contract may be renewed upon the mutual written consent of the Agency, and the Vendor, with approval of the Purchasing Division and the Attorney General's office (Attorney General approval is as to form only). Any request for renewal must be submitted to the Purchasing Division Director thirty (30) days prior to the expiration date of the initial contract term or appropriate renewal term. A Contract renewal shall be in accordance with the terms and conditions of the original contract. Renewal of this Contract is limited to two (2) successive one (1) year periods. Automatic renewal of this Contract is prohibited. Notwithstanding the foregoing, Purchasing Division approval is not required on agency delegated or exempt purchases. Attorney General approval may be required for vendor terms and conditions.

Reasonable Time Extension: At the sole discretion of the Purchasing Division Director, and with approval from the Attorney General's office (Attorney General approval is as to form only), this Contract may be extended for a reasonable time after the initial Contract term or after any renewal term as may be necessary to obtain a new contract or renew this Contract. Any reasonable time extension shall not exceed twelve (12) months. Vendor may avoid a reasonable time extension by providing the Purchasing Division Director with written notice of Vendor's desire to terminate this Contract 30 days prior to the expiration of the then current term. During any reasonable time extension period, the Vendor may terminate this Contract for any reason upon giving the Purchasing Division Director 30 days written notice. Automatic extension of this Contract is prohibited. Notwithstanding the foregoing, Purchasing Division approval is not required on agency delegated or exempt purchases, but Attorney General approval may be required.

Release Order Limitations: In the event that this contract permits release orders, a release order may only be issued during the time this Contract is in effect. Any release order issued within one year of the expiration of this Contract shall be effective for one year from the date the release order is issued. No release order may be extended beyond one year after this Contract has expired.

☐ **Fixed Period Contract:** This Contract becomes effective upon Vendor's receipt of the notice to proceed and must be completed within days.

☐ **One Time Purchase:** The term of this Contract shall run from the issuance of the Purchase Order until all of the goods contracted for have been delivered, but in no event shall this Contract extend for more than one fiscal year.

☐ **Other:** See attached.

4. **NOTICE TO PROCEED:** Vendor shall begin performance of this Contract immediately upon receiving notice to proceed unless otherwise instructed by the Agency. Unless otherwise specified, the fully executed Purchase Order will be considered notice to proceed

5. **QUANTITIES:** The quantities required under this Contract shall be determined in accordance with the category that has been identified as applicable to this Contract below.

☐ **Open End Contract:** Quantities listed in this Solicitation are approximations only, based on estimates supplied by the Agency. It is understood and agreed that the Contract shall cover the quantities actually ordered for delivery during the term of the Contract, whether more or less than the quantities shown.

☐ **Service:** The scope of the service to be provided will be more clearly defined in the specifications included herewith.

☑ **Combined Service and Goods:** The scope of the service and deliverable goods to be provided will be more clearly defined in the specifications included herewith.

☐ **One Time Purchase:** This Contract is for the purchase of a set quantity of goods that are identified in the specifications included herewith. Once those items have been delivered, no additional goods may be procured under this Contract without an appropriate change order approved by the Vendor, Agency, Purchasing Division, and Attorney General's office.

6. **PRICING:** The pricing set forth herein is firm for the life of the Contract, unless specified elsewhere within this Solicitation/Contract by the State. A Vendor's inclusion of price adjustment provisions in its bid, without an express authorization from the State in the Solicitation to do so, may result in bid disqualification.

7. **EMERGENCY PURCHASES:** The Purchasing Division Director may authorize the Agency to purchase goods or services in the open market that Vendor would otherwise provide under this Contract if those goods or services are for immediate or expedited delivery in an emergency. Emergencies shall include, but are not limited to, delays in transportation or an unanticipated increase in the volume of work. An emergency purchase in the open market, approved by the Purchasing Division Director, shall not constitute of breach of this Contract and shall not entitle the Vendor to any form of compensation or damages. This provision does not excuse the State from fulfilling its obligations under a One Time Purchase contract.

8. **REQUIRED DOCUMENTS:** All of the items checked below must be provided to the Purchasing Division by the Vendor as specified below.

☐ **BID BOND:** All Vendors shall furnish a bid bond in the amount of five percent (5%) of the total amount of the bid protecting the State of West Virginia. The bid bond must be submitted with the bid.

☐ **PERFORMANCE BOND:** The apparent successful Vendor shall provide a performance bond in the amount of . The performance bond must be issued and received by the Purchasing Division prior to Contract award. On construction contracts, the performance bond must be 100% of the Contract value.

☐ **LABOR/MATERIAL PAYMENT BOND:** The apparent successful Vendor shall provide a labor/material payment bond in the amount of 100% of the Contract value. The labor/material payment bond must be issued and delivered to the Purchasing Division prior to Contract award.

In lieu of the Bid Bond, Performance Bond, and Labor/Material Payment Bond, the Vendor may provide certified checks, cashier's checks, or irrevocable letters of credit. Any certified check, cashier's check, or irrevocable letter of credit provided in lieu of a bond must be of the same amount and delivered on the same schedule as the bond it replaces. A letter of credit submitted in lieu of a performance and labor/material payment bond will only be allowed for projects under $100,000. Personal or business checks are not acceptable.

☐ **MAINTENANCE BOND:** The apparent successful Vendor shall provide a two (2) year maintenance bond covering the roofing system. The maintenance bond must be issued and delivered to the Purchasing Division prior to Contract award.

☑ **WORKERS' COMPENSATION INSURANCE:** The apparent successful Vendor shall have appropriate workers' compensation insurance and shall provide proof thereof upon request.

☑ **INSURANCE:** The apparent successful Vendor shall furnish proof of the following insurance prior to Contract award and shall list the state as a certificate holder:

☑ **Commercial General Liability Insurance:**
$1,000,000.00 or more.

☐ **Builders Risk Insurance:** builders risk – all risk insurance in an amount equal to 100% of the amount of the Contract.

☐

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The apparent successful Vendor shall also furnish proof of any additional insurance requirements contained in the specifications prior to Contract award regardless of whether or not that insurance requirement is listed above.

☐ **LICENSE(S) / CERTIFICATIONS / PERMITS:** In addition to anything required under the Section entitled Licensing, of the General Terms and Conditions, the apparent successful Vendor shall furnish proof of the following licenses, certifications, and/or permits prior to Contract award, in a form acceptable to the Purchasing Division.

☐

☐

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The apparent successful Vendor shall also furnish proof of any additional licenses or certifications contained in the specifications prior to Contract award regardless of whether or not that requirement is listed above.

9. **LITIGATION BOND:** The Director reserves the right to require any Vendor that files a protest of an award to submit a litigation bond in the amount equal to one percent of the lowest bid submitted or $5,000, whichever is greater. The entire amount of the bond shall be forfeited if the hearing officer determines that the protest was filed for frivolous or improper purpose, including but not limited to, the purpose of harassing, causing unnecessary delay, or needless expense for the Agency. All litigation bonds shall be made payable to the Purchasing Division. In lieu of a bond, the protester may submit a cashier's check or certified check payable to the Purchasing Division. Cashier's or certified checks will be deposited with and held by the State Treasurer's office. If it is determined that the protest has not been filed for frivolous or improper purpose, the bond or deposit shall be returned in its entirety.

10. **ALTERNATES:** Any model, brand, or specification listed herein establishes the acceptable level of quality only and is not intended to reflect a preference for, or in any way favor, a particular brand or vendor. Vendors may bid alternates to a listed model or brand provided that the alternate is at least equal to the model or brand and complies with the required specifications. The equality of any alternate being bid shall be determined by the State at its sole discretion. Any Vendor bidding an alternate model or brand should clearly identify the alternate items in its bid and should include manufacturer's specifications, industry literature, and/or any other relevant documentation demonstrating the equality of the alternate items. Failure to provide information for alternate items may be grounds for rejection of a Vendor's bid.

11. **EXCEPTIONS AND CLARIFICATIONS:** The Solicitation contains the specifications that shall form the basis of a contractual agreement. Vendor shall clearly mark any exceptions, clarifications, or

other proposed modifications in its bid. Exceptions to, clarifications of, or modifications of a requirement or term and condition of the Solicitation may result in bid disqualification.

12. **LIQUIDATED DAMAGES:** Vendor shall pay liquidated damages in the amount for

This clause shall in no way be considered exclusive and shall not limit the State or Agency's right to pursue any other available remedy.

13. **ACCEPTANCE/REJECTION:** The State may accept or reject any bid in whole, or in part. Vendor's signature on its bid signifies acceptance of the terms and conditions contained in the Solicitation and Vendor agrees to be bound by the terms of the Contract, as reflected in the Purchase Order, upon receipt.

14. **REGISTRATION:** Prior to Contract award, the apparent successful Vendor must be properly registered with the West Virginia Purchasing Division and must have paid the $125 fee if applicable.

15. **COMMUNICATION LIMITATIONS:** In accordance with West Virginia Code of State Rules §148-1-6.6, communication with the State of West Virginia or any of its employees regarding this Solicitation during the solicitation, bid, evaluation or award periods, except through the Purchasing Division, is strictly prohibited without prior Purchasing Division approval. Purchasing Division approval for such communication is implied for all agency delegated and exempt purchases.

16. **FUNDING:** This Contract shall continue for the term stated herein, contingent upon funds being appropriated by the Legislature or otherwise being made available. In the event funds are not appropriated or otherwise made available, this Contract becomes void and of no effect beginning on July 1 of the fiscal year for which funding has not been appropriated or otherwise made available.

17. **PAYMENT:** Payment in advance is prohibited under this Contract. Payment may only be made after the delivery and acceptance of goods or services. The Vendor shall submit invoices, in arrears, to the Agency at the address on the face of the purchase order labeled "Invoice To."

18. **UNIT PRICE:** Unit prices shall prevail in cases of a discrepancy in the Vendor's bid.

19. **DELIVERY:** All quotations are considered freight on board destination ("F.O.B. destination") unless alternate shipping terms are clearly identified in the bid. Vendor's listing of shipping terms that contradict the shipping terms expressly required by this Solicitation may result in bid disqualification.

20. **INTEREST:** Interest attributable to late payment will only be permitted if authorized by the West Virginia Code. Presently, there is no provision in the law for interest on late payments.

21. **PREFERENCE:** Vendor Preference may only be granted upon written request and only in accordance with the West Virginia Code § 5A-3-37 and the West Virginia Code of State Rules. A Resident Vendor Certification form has been attached hereto to allow Vendor to apply for the preference. Vendor's

failure to submit the Resident Vendor Certification form with its bid will result in denial of Vendor Preference. Vendor Preference does not apply to construction projects.

22. **SMALL, WOMEN-OWNED, OR MINORITY-OWNED BUSINESSES:** For any solicitations publicly advertised for bid on or after July 1, 2012, in accordance with West Virginia Code §5A-3-37(a)(7) and W. Va. CSR § 148-22-9, any non-resident vendor certified as a small, women-owned, or minority-owned business under W. Va. CSR § 148-22-9 shall be provided the same preference made available to any resident vendor. Any non-resident small, women-owned, or minority-owned business must identify itself as such in writing, must submit that writing to the Purchasing Division with its bid, and must be properly certified under W. Va. CSR § 148-22-9 prior to submission of its bid to receive the preferences made available to resident vendors. Preference for a non-resident small, women-owned, or minority owned business shall be applied in accordance with W. Va. CSR § 148-22-9.

23. **TAXES:** The Vendor shall pay any applicable sales, use, personal property or any other taxes arising out of this Contract and the transactions contemplated thereby. The State of West Virginia is exempt from federal and state taxes and will not pay or reimburse such taxes.

24. **CANCELLATION:** The Purchasing Division Director reserves the right to cancel this Contract immediately upon written notice to the vendor if the materials or workmanship supplied do not conform to the specifications contained in the Contract. The Purchasing Division Director may cancel any purchase or Contract upon 30 days written notice to the Vendor in accordance with West Virginia Code of State Rules § 148-1-7.16.2.

25. **WAIVER OF MINOR IRREGULARITIES:** The Director reserves the right to waive minor irregularities in bids or specifications in accordance with West Virginia Code of State Rules § 148-1-4.6.

26. **TIME:** Time is of the essence with regard to all matters of time and performance in this Contract.

27. **APPLICABLE LAW**: This Contract is governed by and interpreted under West Virginia law without giving effect to its choice of law principles. Any information provided in specification manuals, or any other source, verbal or written, which contradicts or violates the West Virginia Constitution, West Virginia Code or West Virginia Code of State Rules is void and of no effect.

28. **COMPLIANCE**: Vendor shall comply with all applicable federal, state, and local laws, regulations and ordinances. By submitting a bid, Vendors acknowledge that they have reviewed, understand, and will comply with all applicable law.

29. **PREVAILING WAGE:** On any contract for the construction of a public improvement, Vendor and any subcontractors utilized by Vendor shall pay a rate or rates of wages which shall not be less than the fair minimum rate or rates of wages (prevailing wage), as established by the West Virginia Division of Labor under West Virginia Code §§ 21-5A-1 et seq. and available at http://www.sos.wv.gov/administrative-law/wagerates/Pages/default.aspx. Vendor shall be responsible for ensuring compliance with prevailing wage requirements and determining when prevailing wage

requirements are applicable. The required contract provisions contained in West Virginia Code of State Rules § 42-7-3 are specifically incorporated herein by reference.

30. **ARBITRATION:** Any references made to arbitration contained in this Contract, Vendor's bid, or in any American Institute of Architects documents pertaining to this Contract are hereby deleted, void, and of no effect.

31. **MODIFICATIONS**: This writing is the parties' final expression of intent. Notwithstanding anything contained in this Contract to the contrary, no modification of this Contract shall be binding without mutual written consent of the Agency, and the Vendor, with approval of the Purchasing Division and the Attorney General's office (Attorney General approval is as to form only). **No Change shall be implemented by the Vendor until such time as the Vendor receives an approved written change order from the Purchasing Division.**

32. **WAIVER:** The failure of either party to insist upon a strict performance of any of the terms or provision of this Contract, or to exercise any option, right, or remedy herein contained, shall not be construed as a waiver or a relinquishment for the future of such term, provision, option, right, or remedy, but the same shall continue in full force and effect. Any waiver must be expressly stated in writing and signed by the waiving party.

33. **SUBSEQUENT FORMS:** The terms and conditions contained in this Contract shall supersede any and all subsequent terms and conditions which may appear on any form documents submitted by Vendor to the Agency or Purchasing Division such as price lists, order forms, invoices, sales agreements, or maintenance agreements, and includes internet websites or other electronic documents. Acceptance or use of Vendor's forms does not constitute acceptance of the terms and conditions contained thereon.

34. **ASSIGNMENT**: Neither this Contract nor any monies due, or to become due hereunder, may be assigned by the Vendor without the express written consent of the Agency, the Purchasing Division, the Attorney General's office (as to form only), and any other government agency or office that may be required to approve such assignments. Notwithstanding the foregoing, Purchasing Division approval may or may not be required on certain agency delegated or exempt purchases.

35. **WARRANTY**: The Vendor expressly warrants that the goods and/or services covered by this Contract will: (a) conform to the specifications, drawings, samples, or other description furnished or specified by the Agency; (b) be merchantable and fit for the purpose intended; and (c) be free from defect in material and workmanship.

36. **STATE EMPLOYEES:** State employees are not permitted to utilize this Contract for personal use and the Vendor is prohibited from permitting or facilitating the same.

37. **BANKRUPTCY**: In the event the Vendor files for bankruptcy protection, the State of West Virginia may deem this Contract null and void, and terminate this Contract without notice.

38. [RESERVED]

39. **CONFIDENTIALITY**: The Vendor agrees that it will not disclose to anyone, directly or indirectly, any such personally identifiable information or other confidential information gained from the Agency, unless the individual who is the subject of the information consents to the disclosure in writing or the disclosure is made pursuant to the Agency's policies, procedures, and rules. Vendor further agrees to comply with the Confidentiality Policies and Information Security Accountability Requirements, set forth in http://www.state.wv.us/admin/purchase/privacy/default.html.

40. **DISCLOSURE:** Vendor's response to the Solicitation and the resulting Contract are considered public documents and will be disclosed to the public in accordance with the laws, rules, and policies governing the West Virginia Purchasing Division. Those laws include, but are not limited to, the Freedom of Information Act found in West Virginia Code § 29B-1-1 et seq.

    If a Vendor considers any part of its bid to be exempt from public disclosure, Vendor must so indicate by specifically identifying the exempt information, identifying the exemption that applies, providing a detailed justification for the exemption, segregating the exempt information from the general bid information, and submitting the exempt information as part of its bid but in a segregated and clearly identifiable format. Failure to comply with the foregoing requirements will result in public disclosure of the Vendor's bid without further notice. A Vendor's act of marking all or nearly all of its bid as exempt is not sufficient to avoid disclosure and WILL NOT BE HONORED. Vendor's act of marking a bid or any part thereof as "confidential" or "proprietary" is not sufficient to avoid disclosure and WILL NOT BE HONORED. In addition, a legend or other statement indicating that all or substantially all of the bid is exempt from disclosure is not sufficient to avoid disclosure and WILL NOT BE HONORED. Vendor will be required to defend any claimed exemption for nondisclosure in the event of an administrative or judicial challenge to the State's nondisclosure. Vendor must indemnify the State for any costs incurred related to any exemptions claimed by Vendor. Any questions regarding the applicability of the various public records laws should be addressed to your own legal counsel prior to bid submission.

41. **LICENSING:** In accordance with West Virginia Code of State Rules §148-1-6.1.7, Vendor must be licensed and in good standing in accordance with any and all state and local laws and requirements by any state or local agency of West Virginia, including, but not limited to, the West Virginia Secretary of State's Office, the West Virginia Tax Department, West Virginia Insurance Commission, or any other state agency or political subdivision. Upon request, the Vendor must provide all necessary releases to obtain information to enable the Purchasing Division Director or the Agency to verify that the Vendor is licensed and in good standing with the above entities.

42. **ANTITRUST:** In submitting a bid to, signing a contract with, or accepting a Purchase Order from any agency of the State of West Virginia, the Vendor agrees to convey, sell, assign, or transfer to the State of West Virginia all rights, title, and interest in and to all causes of action it may now or hereafter acquire under the antitrust laws of the United States and the State of West Virginia for price fixing and/or unreasonable restraints of trade relating to the particular commodities or services purchased or acquired

by the State of West Virginia. Such assignment shall be made and become effective at the time the purchasing agency tenders the initial payment to Vendor.

43. **VENDOR CERTIFICATIONS:** By signing its bid or entering into this Contract, Vendor certifies (1) that its bid was made without prior understanding, agreement, or connection with any corporation, firm, limited liability company, partnership, person or entity submitting a bid for the same material, supplies, equipment or services; (2) that its bid is in all respects fair and without collusion or fraud; (3) that this Contract is accepted or entered into without any prior understanding, agreement, or connection to any other entity that could be considered a violation of law; and (4) that it has reviewed this RFQ in its entirety, understands the requirements, terms and conditions, and other information contained herein. Vendor's signature on its bid also affirms that neither it nor its representatives have any interest, nor shall acquire any interest, direct or indirect, which would compromise the performance of its services hereunder. Any such interests shall be promptly presented in detail to the Agency.

    The individual signing this bid on behalf of Vendor certifies that he or she is authorized by the Vendor to execute this bid or any documents related thereto on Vendor's behalf; that he or she is authorized to bind the Vendor in a contractual relationship; and that, to the best of his or her knowledge, the Vendor has properly registered with any State agency that may require registration.

44. **PURCHASING CARD ACCEPTANCE:** The State of West Virginia currently utilizes a Purchasing Card program, administered under contract by a banking institution, to process payment for goods and services. The Vendor must accept the State of West Virginia's Purchasing Card for payment of all orders under this Contract unless the box below is checked.

    ☐ Vendor is not required to accept the State of West Virginia's Purchasing Card as payment for all goods and services.

45. **VENDOR RELATIONSHIP:** The relationship of the Vendor to the State shall be that of an independent contractor and no principal-agent relationship or employer-employee relationship is contemplated or created by this Contract. The Vendor as an independent contractor is solely liable for the acts and omissions of its employees and agents. Vendor shall be responsible for selecting, supervising, and compensating any and all individuals employed pursuant to the terms of this Solicitation and resulting contract. Neither the Vendor, nor any employees or subcontractors of the Vendor, shall be deemed to be employees of the State for any purpose whatsoever. Vendor shall be exclusively responsible for payment of employees and contractors for all wages and salaries, taxes, withholding payments, penalties, fees, fringe benefits, professional liability insurance premiums, contributions to insurance and pension, or other deferred compensation plans, including but not limited to, Workers' Compensation and Social Security obligations, licensing fees, *etc.* and the filing of all necessary documents, forms and returns pertinent to all of the foregoing. Vendor shall hold harmless the State, and shall provide the State and Agency with a defense against any and all claims including, but not limited to, the foregoing payments, withholdings, contributions, taxes, Social Security taxes, and employer income tax returns.

46. **INDEMNIFICATION:** The Vendor agrees to indemnify, defend, and hold harmless the State and the Agency, their officers, and employees from and against: (1) Any claims or losses for services rendered

by any subcontractor, person, or firm performing or supplying services, materials, or supplies in connection with the performance of the Contract; (2) Any claims or losses resulting to any person or entity injured or damaged by the Vendor, its officers, employees, or subcontractors by the publication, translation, reproduction, delivery, performance, use, or disposition of any data used under the Contract in a manner not authorized by the Contract, or by Federal or State statutes or regulations; and (3) Any failure of the Vendor, its officers, employees, or subcontractors to observe State and Federal laws including, but not limited to, labor and wage and hour laws.

47. **PURCHASING AFFIDAVIT:** In accordance with West Virginia Code § 5A-3-10a, all Vendors are required to sign, notarize, and submit the Purchasing Affidavit stating that neither the Vendor nor a related party owe a debt to the State in excess of $1,000. The affidavit must be submitted prior to award, but should be submitted with the Vendor's bid. A copy of the Purchasing Affidavit is included herewith.

48. **ADDITIONAL AGENCY AND LOCAL GOVERNMENT USE:** This Contract may be utilized by and extends to other agencies, spending units, and political subdivisions of the State of West Virginia; county, municipal, and other local government bodies; and school districts ("Other Government Entities"). This Contract shall be extended to the aforementioned Other Government Entities on the same prices, terms, and conditions as those offered and agreed to in this Contract. If the Vendor does not wish to extend the prices, terms, and conditions of its bid and subsequent contract to the Other Government Entities, the Vendor must clearly indicate such refusal in its bid. A refusal to extend this Contract to the Other Government Entities shall not impact or influence the award of this Contract in any manner.

49. **CONFLICT OF INTEREST:** Vendor, its officers or members or employees, shall not presently have or acquire any interest, direct or indirect, which would conflict with or compromise the performance of its obligations hereunder. Vendor shall periodically inquire of its officers, members and employees to ensure that a conflict of interest does not arise. Any conflict of interest discovered shall be promptly presented in detail to the Agency.

50. **REPORTS:** Vendor shall provide the Agency and/or the Purchasing Division with the following reports identified by a checked box below:

☐ Such reports as the Agency and/or the Purchasing Division may request. Requested reports may include, but are not limited to, quantities purchased, agencies utilizing the contract, total contract expenditures by agency, etc.

☐ Quarterly reports detailing the total quantity of purchases in units and dollars, along with a listing of purchases by agency. Quarterly reports should be delivered to the Purchasing Division via email at purchasing.requisitions@wv.gov.

51. **BACKGROUND CHECK:** In accordance with W. Va. Code § 15-2D-3, the Director of the Division of Protective Services shall require any service provider whose employees are regularly employed on the grounds or in the buildings of the Capitol complex or who have access to sensitive or critical information

to submit to a fingerprint-based state and federal background inquiry through the state repository. The service provider is responsible for any costs associated with the fingerprint-based state and federal background inquiry.

After the contract for such services has been approved, but before any such employees are permitted to be on the grounds or in the buildings of the Capitol complex or have access to sensitive or critical information, the service provider shall submit a list of all persons who will be physically present and working at the Capitol complex to the Director of the Division of Protective Services for purposes of verifying compliance with this provision.

The State reserves the right to prohibit a service provider's employees from accessing sensitive or critical information or to be present at the Capitol complex based upon results addressed from a criminal background check.

Service providers should contact the West Virginia Division of Protective Services by phone at (304)558-9911 for more information.

52. **PREFERENCE FOR USE OF DOMESTIC STEEL PRODUCTS:** Except when authorized by the Director of the Purchasing Division pursuant to W. Va. Code § 5A-3-56, no contractor may use or supply steel products for a State Contract Project other than those steel products made in the United States. A contractor who uses steel products in violation of this section may be subject to civil penalties pursuant to W. Va. Code § 5A-3-56. As used in this section:

a. "State Contract Project" means any erection or construction of, or any addition to, alteration of or other improvement to any building or structure, including, but not limited to, roads or highways, or the installation of any heating or cooling or ventilating plants or other equipment, or the supply of and materials for such projects, pursuant to a contract with the State of West Virginia for which bids were solicited on or after June 6, 2001.

b. "Steel Products" means products rolled, formed, shaped, drawn, extruded, forged, cast, fabricated or otherwise similarly processed, or processed by a combination of two or more or such operations, from steel made by the open heath, basic oxygen, electric furnace, Bessemer or other steel making process.

The Purchasing Division Director may, in writing, authorize the use of foreign steel products if:

a. The cost for each contract item used does not exceed one tenth of one percent (.1%) of the total contract cost or two thousand five hundred dollars ($2,500.00), whichever is greater. For the purposes of this section, the cost is the value of the steel product as delivered to the project; or

b. The Director of the Purchasing Division determines that specified steel materials are not produced in the United States in sufficient quantity or otherwise are not reasonably available to meet contract requirements.

53. PREFERENCE FOR USE OF DOMESTIC ALUMINUM, GLASS, AND STEEL: In Accordance with W. Va. Code § 5-19-1 et seq., and W. Va. CSR § 148-10-1 et seq., for every contract or subcontract, subject to the limitations contained herein, for the construction, reconstruction, alteration, repair, improvement or maintenance of public works or for the purchase of any item of machinery or equipment to be used at sites of public works, only domestic aluminum, glass or steel products shall be supplied unless the spending officer determines, in writing, after the receipt of offers or bids, (1) that the cost of domestic aluminum, glass or steel products is unreasonable or inconsistent with the public interest of the State of West Virginia, (2) that domestic aluminum, glass or steel products are not produced in sufficient quantities to meet the contract requirements, or (3) the available domestic aluminum, glass, or steel do not meet the contract specifications. This provision only applies to public works contracts awarded in an amount more than fifty thousand dollars ($50,000) or public works contracts that require more than ten thousand pounds of steel products.

The cost of domestic aluminum, glass, or steel products may be unreasonable if the cost is more than twenty percent (20%) of the bid or offered price for foreign made aluminum, glass, or steel products. If the domestic aluminum, glass or steel products to be supplied or produced in a "substantial labor surplus area", as defined by the United States Department of Labor, the cost of domestic aluminum, glass, or steel products may be unreasonable if the cost is more than thirty percent (30%) of the bid or offered price for foreign made aluminum, glass, or steel products.

This preference shall be applied to an item of machinery or equipment, as indicated above, when the item is a single unit of equipment or machinery manufactured primarily of aluminum, glass or steel, is part of a public works contract and has the sole purpose or of being a permanent part of a single public works project. This provision does not apply to equipment or machinery purchased by a spending unit for use by that spending unit and not as part of a single public works project.

All bids and offers including domestic aluminum, glass or steel products that exceed bid or offer prices including foreign aluminum, glass or steel products after application of the preferences provided in this provision may be reduced to a price equal to or lower than the lowest bid or offer price for foreign aluminum, glass or steel products plus the applicable preference. If the reduced bid or offer prices are made in writing and supersede the prior bid or offer prices, all bids or offers, including the reduced bid or offer prices, will be reevaluated in accordance with this rule.

SPECIFICATIONS

1. **PURPOSE AND SCOPE:** The West Virginia Purchasing Division is soliciting bids on behalf of the West Virginia Educational Broadcasting Authority (EBA) to establish a contract for the one time purchase of site-to-site connectivity between three properties of the EBA and two West Virginia Network (WVNet) locations, as well as Internet access. This will be a 3-year contract.

   The connectivity (see exhibit B) will be used as follows:

   - Layer 2 Ethernet:
     - Inter-office data and file exchange
     - Connection to the State of WV backbone
     - Teleconferencing
     - Internal video streaming
     - Content production sharing and viewing / listening
     - Equipment monitoring, including microwave systems
     - Radio broadcast and monitoring
     - Disaster recovery
     - Testing of emerging technologies to transport broadcast video over layer 2 Ethernet

   - Digital Signal 3 (DS3):
     - Transport of broadcast video to transmitters
     - Transport of Production video feeds between locations
     - Transport of live broadcasts to our Master Control
     - Failover capabilities for broadcast video

   - Internet Access:
     - Audio and Video streaming of current and archived content
     - Delivery of educational content to appropriate parties
     - Remote access for news reporters – report from the field
     - Remote access for technical staff – remote monitoring and repair from the field
     - Failover connections between locations in the event of site-to-site connectivity failures
     - General Internet Access

2. **DEFINITIONS:** The terms listed below shall have the meanings assigned to them below. Additional definitions can be found in section 2 of the General Terms and Conditions.

   2.1 "Contract Item" means:

2.1.1 **LAYER 2 ETHERNET:** Ethernet connectivity as defined by the IEEE (Institute of Electrical and Electronics Engineers) 802.3 standard and all updates to the standard regarding wired circuits.

2.1.2 **CLEAR CHANNEL DIGITAL SIGNAL 3 (DS3) CIRCUIT:** Point-to-Point, full duplex, clear channel carrier meeting ITU-T (International Telecommunication Union – Telecommunication Standardization Sector) G.703 specifications.

2.1.3 **INTERNET ACCESS:** Point-of-Presence (POP) connecting Local Area Networks (LANs) to the public Internet.

2.2 **"Pricing Page"** means the pages upon which Vendor should list its proposed price for the Contract Items in the manner requested. The Pricing Page is attached hereto as Exhibit A.

2.3 **"RFQ"** means the official request for quotation published by the Purchasing Division and identified as EBA471A.

2.4 **"QUALITY OF SERVICE (QOS)":** Quality of Service as defined by the IEEE 802.1Q standard for priority level tagging within an Ethernet frame header.

2.5 **"REVERSE DNS (DOMAIN NAME SYSTEM)":** means reverse DNS lookup or reverse DNS resolution. It is the determination of a domain name that is associated with a given IP address using the Domain Name System of the Internet.

2.6 **"NODE"** means a piece of equipment through which a circuit traverses creating an additional point of failure.

2.7 **"Point of Demarcation"** means the point at which responsibility for the circuits and hardware changes from the vendor to the EBA.

3. GENERAL REQUIREMENTS:

3.1 **Mandatory Pre-Bid Meetings:** There shall be a pre-bid meeting at the Beckley offices of the EBA (124 Industrial Park Rd., Beaver WV 25813) on 05/07/2014 at 10:30 a.m. The purpose of this meeting is to discuss the contract, answer any questions vendors may have, and permit vendors to tour the facility in order to determine accurate build-out costs. There shall be a second pre-bid meeting at the Charleston offices of the EBA (600 Capitol St., Charleston, WV 25301) on 05/08/2014 at 10:30 a.m. There shall be a third pre-bid meeting at the Morgantown

offices of the EBA (191 Scott Ave., Morgantown, WV 26505) on 05/09/2014 at 11:00 a.m. The sole purpose of the second and third meetings is to tour the facilities in order to determine accurate build-out costs. Any vendor wishing to bid on this contract must attend all pre-bid meetings.

3.2 Subcontracting: The vendor must own all fiber, copper wire, and equipment, and all workers must be direct employees of the vendor with the exception of approved subcontractors as defined below.

3.2.1 Vendor shall be wholly responsible for any subcontracted services, including but not limited to: safety, insurance, training, quality assurance, response time, and oversight.

3.2.2 All subcontracting must be approved by the EBA prior to proceeding. Credentials and references for any proposed subcontractors shall be provided to the WV Purchasing Division within 24 hours after bid opening.

3.3 All Inclusive: Vendor must be able to provide all items and options on this RFQ to be eligible for this contract.

3.4 Mandatory Contract Item Requirements: Contract Items must meet or exceed the mandatory requirements listed below.

3.4.1 LAYER 2 ETHERNET

3.4.1.1 Circuits must meet all IEEE standards for Ethernet over wired circuits.

3.4.1.2 Vendor must have redundant paths for the layer 2 Ethernet circuits on its core network such that a line cut, or similar issue, will automatically failover to another path with no service interruption. The vendor shall provide a basic diagram of their core network illustrating this redundancy. This diagram must illustrate that there is no single point of failure and be acceptable to the EBA. The connection from the vendor's core network to the EBA's sites may be non-redundant.

3.4.1.3 Ethernet circuit shall traverse a maximum of 20 nodes from point of origin to point of termination. Vendor shall supply a list of these nodes.

3.4.1.4 Circuits must be compatible with all switches, routers, and other equipment using standard layer 2 Ethernet technologies.

3.4.1.5 Vendor must honor all EBA Quality-of-Service (QoS) assignments across the vendor's entire network. These designations must apply even when the EBA is sharing bandwidth with other vendor customers.

3.4.1.6 Vendor must segregate the provided 1 Gigabit Ethernet circuits into multiple RJ-45 ports of varying bandwidth and purpose. Bandwidth shall be independently guaranteed to be a minimum of stated bandwidth on all ports, with no traffic on any port affecting traffic on another port. Initial segregation will be as described in Exhibit C, Ethernet Segregation. Vendor shall, on request by the EBA, but not to exceed 1 time in a 6-month period, reconfigure this segregation at no charge. The point of demarcation shall be these ports.

3.4.2 DIGITAL SIGNAL 3 (DS3) CIRCUIT

3.4.2.1 DS3 must meet all ITU-T specifications for G.703 circuits. See Exhibits D through G.

3.4.2.2 DS3 must be configured with CBIT framing as described in Exhibit H, Fundamentals of DS3, published by Telecommunications Techniques Corporation.

3.4.2.3 Vendor must supply timing for the DS3 circuit.

3.4.2.4 DS3 circuits must be full duplex; permitting separate data streams each direction.

3.4.2.5 DS3 circuits must terminate in 2 BNC video type connections; 1 transmit connection and 1 receive connection. These connections shall be the point of demarcation.

3.4.2.6 Each EBA site may be the terminating point for two DS3 circuits (see Exhibit B). At each site each DS3 shall be routed such that no single failure on the vendor's core network will bring down both DS3 circuits. The vendor shall provide a basic diagram of their core network illustrating this. This diagram must illustrate that there is no single point of failure and be acceptable to the EBA. The connection from the vendor's core network to the EBA's sites may be non-redundant.

3.4.2.7 DS3 circuits shall traverse a maximum of 20 nodes from point of origin to point of termination. Vendor shall supply a list of these nodes.

3.4.3 INTERNET CONNECTIVITY

3.4.3.1 Internet connections must be full duplex; stated bandwidth both directions.

3.4.3.2 Vendor must assign a class C subnet of 256 public IP numbers (minimum) for use by the EBA. Reverse DNS (Domain Name System) configurations for this subnet will be maintained by the EBA with the Vendor transferring this information to its own servers via zone transfers.

3.4.3.3 Vendor must support eBGP (external Border Gateway Protocol) for failover of public IP traffic to a 3rd party's Internet service.

3.4.3.3.1 Vendor must cooperate / coordinate with any parties necessary to configure and test these failover capabilities.

3.4.3.3.2 For failover purposes, vendor must permit the 3rd party Internet provider to announce all vendor-owned public IP's assigned to the EBA.

3.4.3.3.3 Upon completion of circuits and notification by the EBA, vendor will configure this failover in a timely manner.

3.5 **Service Level Commitments:** Vendor shall price their circuits such that they shall meet all the following requirements:

3.5.1 Monitoring:

3.5.1.1 Vendor should monitor all circuits for latency, packet loss, and up time. Any available statistics shall be provided to the EBA with their monthly invoice showing the average latency, percentage packet loss, and percentage up time for the billing cycle. If available, these statistics will also be provided to the EBA for any time period upon request. If vendor is unable to monitor any of these service specifications, the vendor will accept the statistics resulting from the EBA's own monitoring.

3.5.1.2 If statistics provided by vendor differ from those resulting from the EBA's own monitoring, vendor shall work with the EBA to determine which statistics are accurate. These agreed-upon statistics shall be used to determine if service level commitments are met. If an agreement cannot be reached, the statistics from the EBA's monitoring shall be used to determine if service level commitments are met.

3.5.2 **Latency:** all circuits must have a maximum of 76 milliseconds of network latency (one-way delay).

3.5.3 **Packet Loss:** Packet delivery is the transit of packets between points of demarcation on the vendor's network. Packet loss is the percentage of packets not reaching their destination. This shall be calculated as ((total forwarded packets – total received packets) / total forwarded packets) x 100. Packet loss must be a maximum of 0.1% when usage on a circuit is less than 100% of its stated bandwidth.

3.5.4 **Bandwidth:** all circuits must perform at their stated bandwidth or higher at all times.

3.5.5 **Target Circuit Availability:** all circuits must have a minimum target circuit availability of 99.99%.

3.5.6 **Mean Time to Repair:** all circuits must have a maximum mean time to repair of 4 hours. Time to repair shall begin when the EBA reports the problem to the vendor and end when the vendor notifies the EBA the repair is complete. Repair completion must be verified by the EBA to be considered final.

3.5.7 **Centralized Point of Contacts:** The vendor shall provide one point of contact for all trouble, repair, and performance issues; and one point of contact for all billing and financial issues. Each point of contact shall be the appropriate party without multiple transfers to resolve issues. The vendor may provide a web portal as an additional means of monitoring, reviewing, and reporting issues.

3.5.8 **Service Level Credits:**

3.5.8.1 If a circuit is down for more than an hour three times or more in any 30 calendar day period vendor shall credit the EBA one month's charges for that circuit.

3.5.8.2 If the mean time to repair is more than 4 hours for any circuit in any 12-month period, vendor shall credit the EBA 10% of the monthly cost of the circuit plus 10% for each additional hour over 5 hours. Fifteen minutes or more shall constitute an additional hour for these calculations. The credit shall not exceed the monthly cost of the circuit.

3.5.8.3 If a circuit doesn't meet the latency or packet loss commitments as described in sections 3.5.2 and 3.5.3, the vendor shall credit the EBA 25% of the monthly cost of the circuit until such time as these commitments are met.

3.5.8.4 If a circuit fails to perform at its stated bandwidth vendor shall reduce the daily costs on the circuit by the same percentage as the bandwidth deficiency. For example: if a Gigabit Ethernet circuit performs at 900 Mb instead of 1000 Mb, it is performing at a 10% deficiency, and would require a 10% daily credit. This credit shall be provided until bandwidth issues are resolved, as documented through trouble tickets.

3.5.8.5 The EBA must request applicable credits within 30 calendar days of receiving the invoice for the billing cycle in which the applicable event occurred.

3.5.8.6 Credits shall never exceed the monthly cost of the circuit in any billing cycle.

3.5.8.7 Credits shall never exceed 25% of the yearly cost of the circuit for any contract year.

3.5.8.8 Vendor will not be responsible for failures to meet Service Level Commitments under the following conditions: (a) interruptions or delays due to failure by the EBA to release services for testing and/or repair; (b) failure of power or equipment for which the

EBA is responsible; (c) delays caused by the EBA not providing timely access to the premises at which the circuits terminate; (d) interruptions or delays as a result of authorized maintenance by the EBA.

4. CONTRACT AWARD:

4.1 Contract Award: The Contract is intended to provide the EBA with a purchase price for the Contract Items. The Contract shall be awarded to the Vendor that provides the Contract Items meeting the required specifications for the lowest overall total cost as shown on the Pricing Pages (Exhibit A).

4.2 Pricing Pages: Vendor should complete the Pricing Pages (Exhibit A) by filling in the appropriate spaces in each column. Vendor should complete the Pricing Page in full as failure to complete the Pricing Pages in their entirety may result in Vendor's bid being disqualified.

Vendor should type or electronically enter the information into the Pricing Pages to prevent errors in the evaluation.

Costs must include ALL charges, including any fees, government surcharges, taxes, travel, or any other charge associated with the service. The vendor will only be paid what is on the Pricing Pages.

Price of options shall be a factor in determining the winning bidder on this RFQ.

Vendor must allow the EBA to order any option at the quoted cost any time during the first 12 months of this contract. Such orders would be an addendum to the primary order, and would expire concurrently.

Notwithstanding the foregoing, the Purchasing Division may correct errors as it deems appropriate.

5. DELIVERY AND RETURN:

5.1 Shipment and Delivery/Installation:

5.1.1 Vendor shall commence installation of the Contract Items immediately after being awarded this Contract and receiving a purchase order or notice to proceed. Vendor shall complete installation of the Contract Items within 45 working days after receiving a purchase order or notice to proceed. Contract Items must be delivered / installed to the EBA at the locations listed on the Pricing Pages (exhibit A). The EBA shall not be responsible for any damage, theft, or loss of equipment or other materials belonging to the vendor during the period of installation.

5.1.2 Verification of Installation: The EBA shall have 60 days from the time circuits are installed and functioning to test all circuits. If all circuits test successfully, monthly billing shall commence at the end of this 60-day test period. If any circuit fails to meet requirements or function as needed, the vendor will have 45 days to remedy the situation. If the vendor fails remediation, the EBA may, at its own discretion, cancel the contract with no penalty. In this situation the EBA may only be charged a maximum of the non-recurring charges (NRC's) listed on the pricing page. If the vendor remedies the situation, monthly billing will commence on the date of remedy.

5.2 Late Delivery/Installation: The EBA must be notified in writing if the delivery/installation of the Contract Items will be delayed for any reason. Any delay in delivery/installation that could cause harm to the EBA will be grounds for cancellation of the Contract, and/or obtaining the Contract Items from a third party.

Any Agency seeking to obtain the Contract Items from a third party under this provision must first obtain approval of the Purchasing Division.

5.3 Delivery Payment/Risk of Loss: Vendor shall deliver the Contract Items F.O.B. destination to the EBA's locations.

5.4 Return of Unacceptable Items: If the EBA deems the Contract Items to be unacceptable, the Contract Items shall be returned to Vendor at Vendor's expense and with no restocking charge. Vendor shall either make arrangements for the return within five (5) days of being notified that items are unacceptable, or permit the EBA to arrange for the return and reimburse the EBA for delivery expenses. If the original packaging cannot be utilized for the return, Vendor will supply the

EBA with appropriate return packaging upon request. All returns of unacceptable items shall be F.O.B. the EBA's locations. The returned product shall either be replaced, or the EBA shall receive a full credit or refund for the purchase price, at the EBA's discretion.

5.5 **Return Due to Agency Error**: Items ordered in error by the EBA will be returned for credit within 30 days of receipt, F.O.B. Vendor's location. Vendor shall not charge a restocking fee if returned products are in a resalable condition. Items shall be deemed to be in a resalable condition if they are unused and in the original packaging. Any restocking fee for items not in a resalable condition shall be the lower of the Vendor's customary restocking fee or 5% of the total invoiced value of the returned items.

6. **PERFORMANCE:** Vendor and the EBA shall agree upon a schedule for performance of Contract Services and Contract Services Deliverables, unless such a schedule is already included herein by the EBA. In the event that this Contract is designated as an open-end contract, Vendor shall perform in accordance with the release orders that may be issued against this Contract.

7. **PAYMENT:** the EBA shall pay the non-recurring charges and monthly rates, as shown on the Pricing Pages (Exhibit A), for all Contract Services performed and accepted under this Contract. Vendor shall accept payment in accordance with the payment procedures of the State of West Virginia.

8. **TRAVEL:** Vendor shall be responsible for all mileage and travel costs, including travel time, associated with performance of this Contract. Any anticipated mileage or travel costs may be included in the flat fee or hourly rate listed on Vendor's bid, but such costs will not be paid by the EBA separately.

9. **FACILITIES ACCESS:** Performance of Contract Services may require access cards and/or keys to gain entrance to the EBA's facilities. In the event that access cards and/or keys are required:

   9.1 Vendor must identify principal service personnel which will be issued access cards and/or keys to perform service.

   9.2 Vendor will be responsible for controlling cards and keys and will pay replacement fee, if the cards or keys become lost or stolen.

9.3 Vendor shall notify the EBA immediately of any lost, stolen, or missing card or key.

9.4 Anyone performing under this Contract will be subject to the EBA's security protocol and procedures.

9.5 Vendor shall inform all staff of the EBA's security protocol and procedures.

10 VENDOR DEFAULT:

10.1 The following shall be considered a vendor default under this Contract.

10.1.1 Failure to perform Contract Services in accordance with the requirements contained herein.

10.1.2 Failure to comply with other specifications and requirements contained herein.

10.1.3 Failure to comply with any laws, rules, and ordinances applicable to the Contract Services provided under this Contract.

10.1.4 Failure to remedy deficient performance upon request.

10.2 The following remedies shall be available to the EBA upon default.

10.2.1 Cancellation of the Contract.

10.2.2 Cancellation of one or more release orders issued under this Contract.

10.2.3 Any other remedies available in law or equity.

RFQ EBA 471A - Appendix
(Items related to the Floor Diagrams)

Appendix 1 - For each of the WV PBS locations does WV PBS require separate entrances into the facilities for the DS3 and Ethernet transports?

*** **No. We require that the DS3 in Beckley terminate in a separate room from the Ethernet ports. Also, Vendor must be responsible for all cabling / wiring / fiber to the point of termination for all circuits. This means Vendor is responsible for troubleshooting and repair all the way to these terminating ports, as described in the RFQ. It is also understood that WV PBS (the EBA) will be responsible for the cost of repair for the portion of Vendor circuits that are inside the EBA premises if they suffer damage, beyond normal wear and tear, not caused by the Vendor.**

Appendix 2 - In each WV PBS demarcation does WV PBS require the carrier to provide a network rack for carrier access equipment or will WV PBS provide their own network rack for the carrier?

*** **The EBA will provide either rack space in existing racks or a separate rack as required.**

Appendix 3 - Can WV PBS provide the carrier a building diagram with desired route of carrier cabling and distance measurements from building penetration point to desired demarcation?

*** **Yes. See attached.**

Appendix 4 - Does WV PBS have Generator and UPS at each WV PBS location?

*** **The EBA has UPS's with generator backups in Charleston and Beckley. Morgantown currently has a UPS, and we are in the process of installing a backup generator.**

Appendix 5 - For each WV PBS location can WV PBS provide EMT conduit or plenum rated innerduct from the interior desired demarcation point inside of the building to the exterior point of entry?

*** **Vendor must provide all EMT conduit or plenum rated innerduct necessary to install these circuits. The EBA will provide any construction necessary to install these, but Vendor must bear the cost of this construction.**

Appendix 6 - Can WV PBS provide dedicated power service to carrier access equipment at the desired WV PBS demarcation point?

*** **Yes.**

Appendix 7 - Does WV PBS have any issues with the carrier that wins the bid using an alternate entry point of the building to reach the specified demarcation points of the interior of the buildings from what is existing today?

*** **For the purposes of determining contract costs, Vendor must use paths as they are detailed in the attached diagrams. We are willing to discuss different routes with the winning bidder, however, if they wish to use an alternate path, they will be responsible for all additional costs and shall not pass these to the EBA.**

Appendix 8 - Does WV PBS require to have a separate physical interface for each LAN specified in Exhibit C – Ethernet Segregation in the Request for Quotation?

*** **Yes, as described in section 3.4.1.6.**

Appendix 9 - Several points of clarification have arisen in relation to room numbers and distances inside the facilities. For the sake of accuracy will you please provide diagrams with room numbers if available and the details and distances for the circuit paths into the building and along the internally provided paths to the locations where the circuit delivery is required for each site?

*** **Yes. See attached. Please note: as the City of Charleston owns the property immediately adjacent to our Charleston facility, we can only provide measurements beginning from our outside wall. We have no access to, or information on, the conduits / cabling under the City sidewalks and streets.**

Appendix 10 - We request clarification on your definition of a "node". Will a piece of equipment be counted as a node if the equipment has multiple layers of protection and therefore does not present a single point of failure?

*** **Yes. Each piece of equipment will constitute a node, even if it has multiple layers of protection. However, if two identical pieces of equipment were configured as a "failover pair", they would be considered one node. A failover pair consists of two pieces of identical equipment that are connected and configured such that any failure on one unit is automatically compensated for on the second unit. Traditionally both units are in the same rack.**

Appendix 11 - The total amount of bandwidth requested provides 1 Gigabit of throughput; we assume this does not count overhead; please clarify.

*** **The 1 Gigabit of throughput does not include overhead. If any overhead is necessary to provide this throughput, the circuit will have to be provisioned with enough bandwidth to accommodate the overhead plus the 1 Gigabit of throughput.**

Appendix 12 - Please clarify that Section 3.2 only applies to work done on EBA premises.

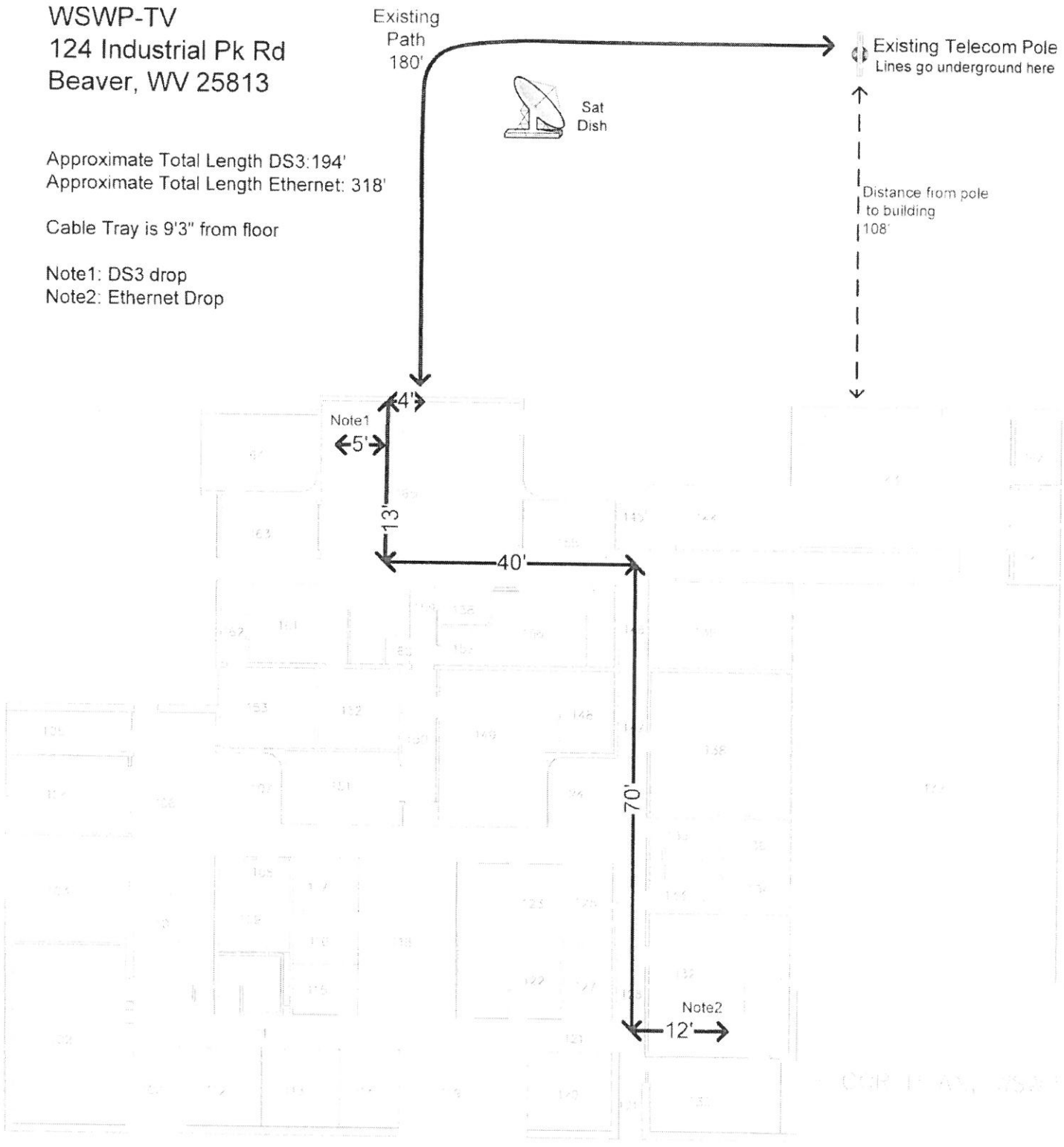
*** **Section 3.2 applies to any subcontracting relating to this contract whether it is on EBA premises or not. Our primary concern with off-premise subcontractors is in relation to the circuits themselves, day-to-day operational and service personnel, and associated equipment and services. If you wish to limit your response to on-premise subcontractors and only those off-premise subcontractors who will be involved in this contract in an ongoing basis, that would be sufficient for us.**

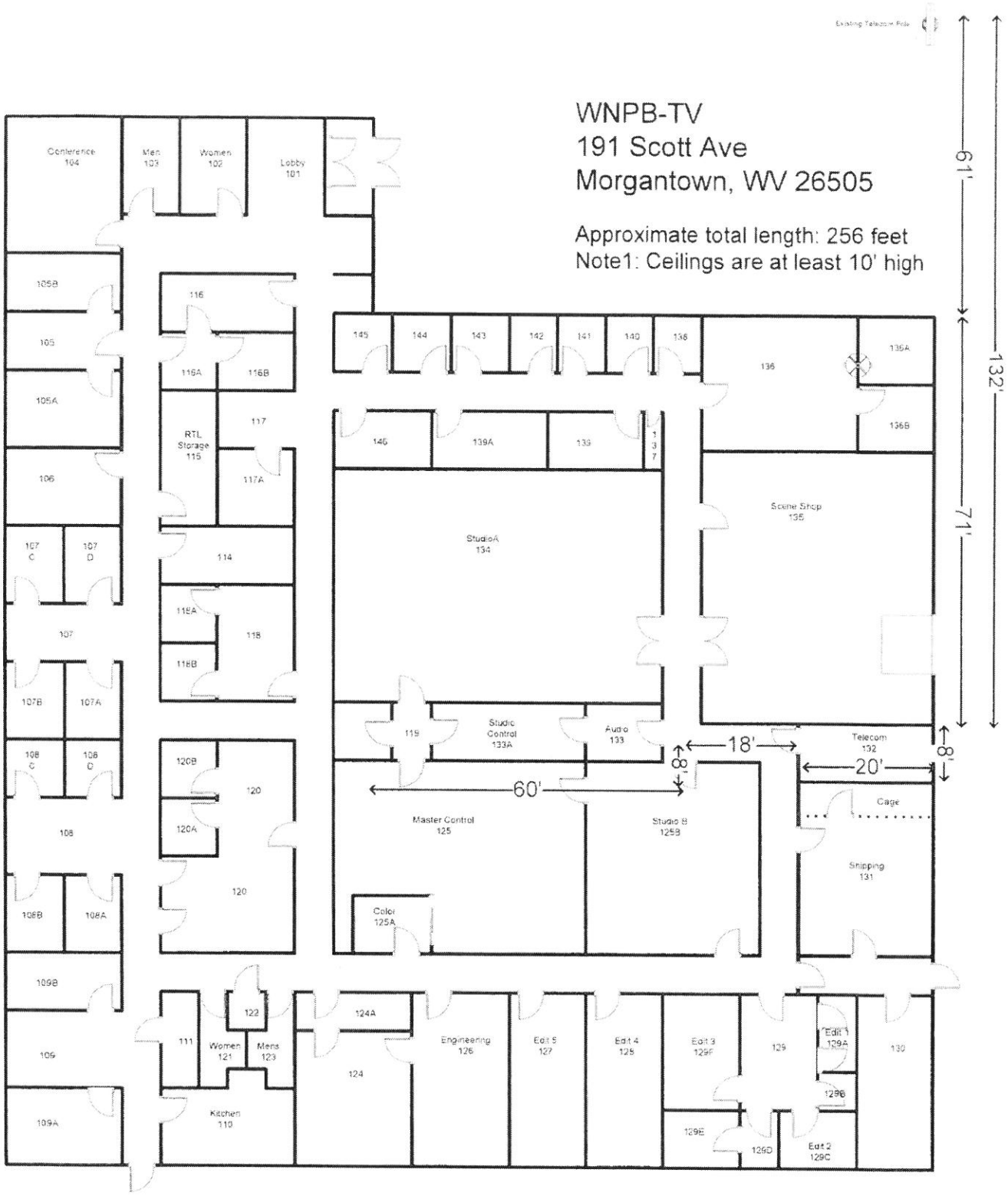
WSWP-TV
124 Industrial Pk Rd
Beaver, WV 25813

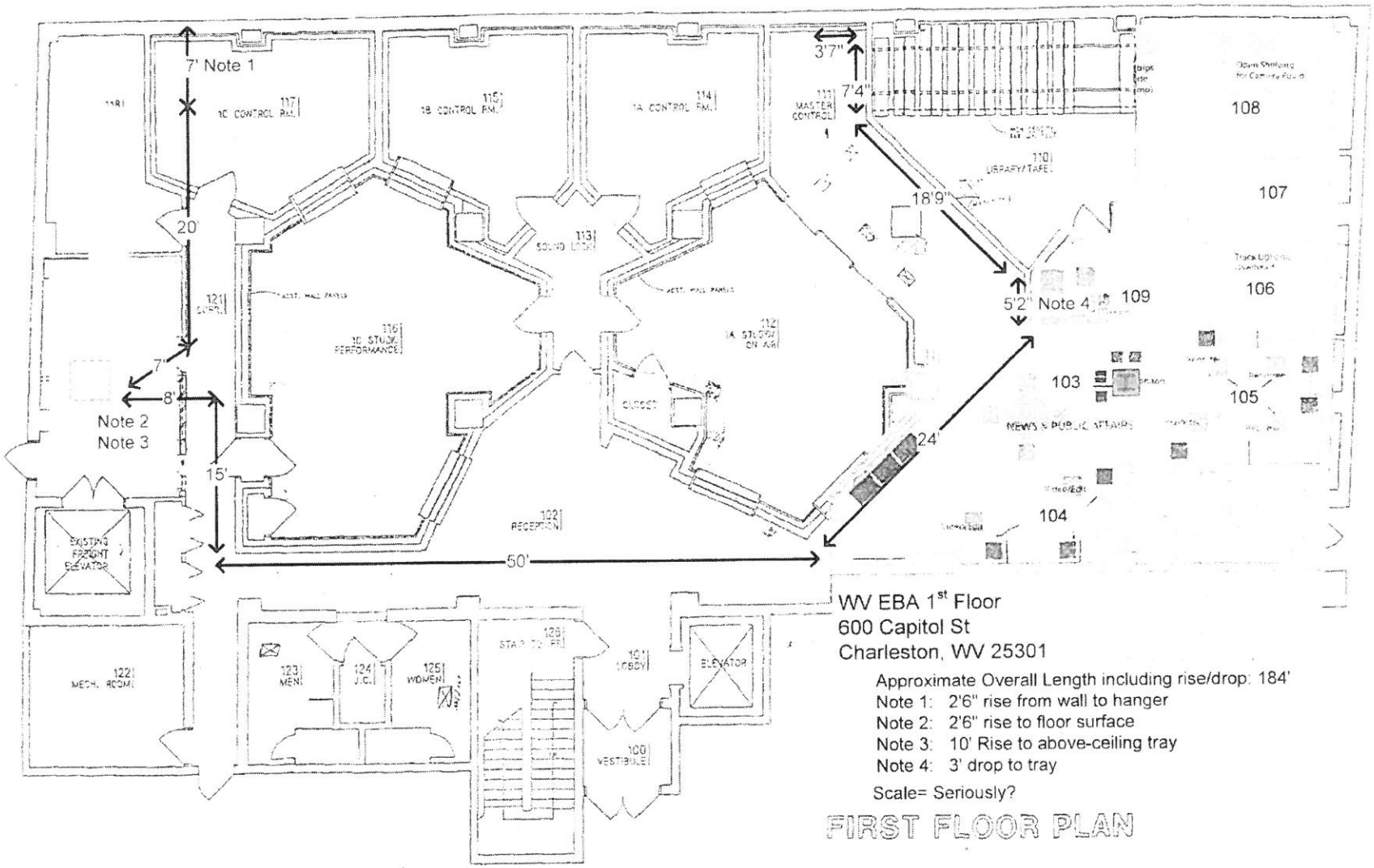
Approximate Total Length DS3:194'
Approximate Total Length Ethernet: 318'

Cable Tray is 9'3" from floor

Note1: DS3 drop
Note2: Ethernet Drop




WNPB-TV
191 Scott Ave
Morgantown, WV 26505
Approximate total length: 256 feet
Note1: Ceilings are at least 10' high
Existing Telecom Pole
61'
71'
132'
18'
8'
20'
8'
60'
Conference 104
Men 103
Women 102
Lobby 101
105B
105
105A
106
107 C
107 D
107
107B
107A
108 C
108 D
108
108B
108A
109B
109
109A
116
116A
116B
117
RTL Storage 115
117A
114
118A
118
118B
120B
120
120A
120
122
111
Women 121
Mens 123
Kitchen 110
124A
124
Engineering 126
Edit 5 127
Edit 4 125
Edit 3 129F
129
Edit 1 129A
130
129B
129E
129D
Edit 2 129C
145
144
143
142
141
140
138
136
136A
136B
146
139A
139
137
Scene Shop 135
Studio A 134
119
Studio Control 133A
Audio 133
Telecom 132
Cage
Shipping 131
Master Control 125
Studio B 125B
Color 125A



WV EBA 1st Floor
600 Capitol St
Charleston, WV 25301

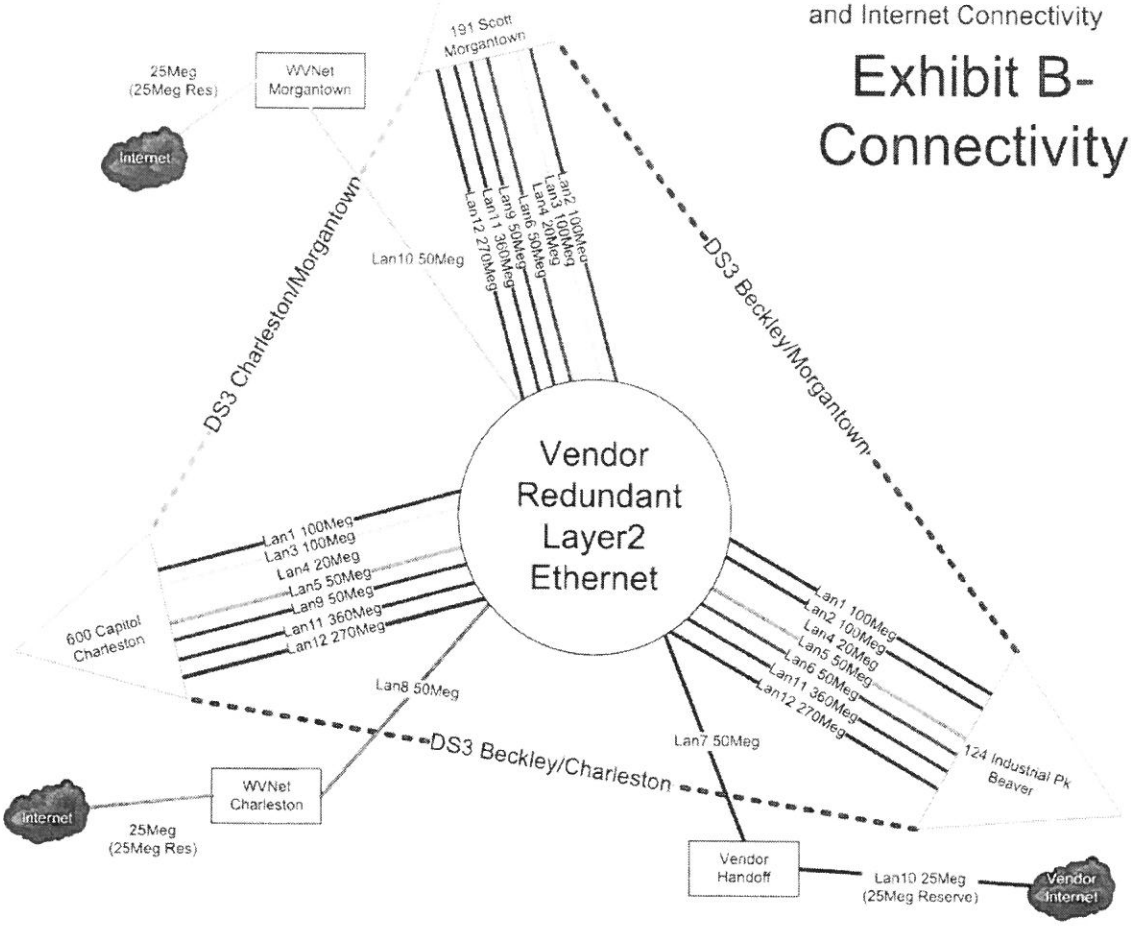
Approximate Overall Length including rise/drop: 184'
Note 1: 2'6" rise from wall to hanger
Note 2: 2'6" rise to floor surface
Note 3: 10' Rise to above-ceiling tray
Note 4: 3' drop to tray

Scale= Seriously?

FIRST FLOOR PLAN

REQUEST FOR QUOTATION
EBA471A WV EBA Site-to-Site
and Internet Connectivity

Exhibit B-Connectivity



EBA471A - Exhibit C -Ethernet Segregation

1 Gig Ethernet Segegration	
Location	**Segegration**
Beckley	LAN 1 - 100 Meg Port LAN 2 - 100 Meg Port LAN 4 – 20 Meg Port LAN 5 - 50 Meg Port LAN 6 - 50 Meg Port LAN 7 - 50 Meg Port to Vendor Internet LAN 11 – 360 Meg Port LAN 12 – 270 Meg Port
Charleston	LAN 1 - 100 Meg Port LAN 3 - 100 Meg Port LAN 4 – 20 Meg Port LAN 5 - 50 Meg Port LAN 8 – 50 Meg Port to WVNet Charleston LAN 9 - 50 Meg Port LAN 11 – 360 Meg Port LAN 12 – 270 Meg Port
Morgantown	LAN 2 - 100 Meg Port LAN 3 - 100 Meg Port LAN 4 – 20 Meg Port LAN 6 - 50 Meg Port LAN 9 - 50 Meg Port LAN 10 – 50 Meg Port – WVNet Morgantown LAN 11 – 360 Meg Port LAN 12 – 270 Meg Port

Segregation of 1 Gig Ethernet Circuits: each 1 Gig Ethernet circuit is to be initially segregated into the 9 ports listed above. Segregation shall be done such that equipment attached to a port at one location shall be connected to equipment at the other sites when connected to the ports with the equivalent designation. For example: if a piece of equipment is connected to the port designated "LAN 1" in Beckley, it will communicate with equipment connected to the "LAN 1" ports in Morgantown and Charleston, but not to equipment on other ports. See Exhibit B. Costs for the port segregation and the connections to WVNet must be included in the overall cost of the 1 Gig layer 2 Ethernet Circuit.

* 50 Meg circuit tto WVNet Morgantown is to terminate at their Morgantown location; West Virginia Network, 837 Chestnut Ridge Road, Morgantown, WV 26505. 50 Meg circuit to WVNet Charleston is to terminate at their Charleston location; WV State Capitol, 1900 Kanawha Blvd East, Bldg 6, 1st Floor, Communications Vault. Any questions concerning these locations may be addressed with Allen Daugherty, West Virginia Network, 837 Chestnut Ridge Road, Morgantown, WV 26505. Phone: 304-293-5192 x 242. Email: allen@mail.wvnet.edu.

EXHIBIT D

INTERNATIONAL TELECOMMUNICATION UNION

ITU-T

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

G.703

(11/2001)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital terminal equipments – General

Physical/electrical characteristics of hierarchical digital interfaces

ITU-T Recommendation G.703

ITU-T G-SERIES RECOMMENDATIONS

TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

INTERNATIONAL TELEPHONE CONNECTIONS AND CIRCUITS	G.100–G.199
GENERAL CHARACTERISTICS COMMON TO ALL ANALOGUE CARRIER-TRANSMISSION SYSTEMS	G.200–G.299
INDIVIDUAL CHARACTERISTICS OF INTERNATIONAL CARRIER TELEPHONE SYSTEMS ON METALLIC LINES	G.300–G.399
GENERAL CHARACTERISTICS OF INTERNATIONAL CARRIER TELEPHONE SYSTEMS ON RADIO-RELAY OR SATELLITE LINKS AND INTERCONNECTION WITH METALLIC LINES	G.400–G.449
COORDINATION OF RADIOTELEPHONY AND LINE TELEPHONY	G.450–G.499
TESTING EQUIPMENTS	G.500–G.599
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DIGITAL TERMINAL EQUIPMENTS	G.700–G.799
General	**G.700–G.709**
Coding of analogue signals by pulse code modulation	G.710–G.719
Coding of analogue signals by methods other than PCM	G.720–G.729
Principal characteristics of primary multiplex equipment	G.730–G.739
Principal characteristics of second order multiplex equipment	G.740–G.749
Principal characteristics of higher order multiplex equipment	G.750–G.759
Principal characteristics of transcoder and digital multiplication equipment	G.760–G.769
Operations, administration and maintenance features of transmission equipment	G.770–G.779
Principal characteristics of multiplexing equipment for the synchronous digital hierarchy	G.780–G.789
Other terminal equipment	G.790–G.799
DIGITAL NETWORKS	G.800–G.899
DIGITAL SECTIONS AND DIGITAL LINE SYSTEM	G.900–G.999
QUALITY OF SERVICE AND PERFORMANCE	G.1000–G.1999
TRANSMISSION MEDIA CHARACTERISTICS	G.6000–G.6999
DIGITAL TERMINAL EQUIPMENTS	G.7000–G.7999
DIGITAL NETWORKS	G.8000–G.8999

For further details, please refer to the list of ITU-T Recommendations.

ITU-T Recommendation G.703

Physical/electrical characteristics of hierarchical digital interfaces

Summary

This Recommendation specifies the recommended physical and electrical characteristics of the interfaces at hierarchical bit rates as described in ITU-T Recs. G.702 (PDH) and G.707 (SDH). The interfaces are defined in terms of general characteristics, specifications at the output ports and input ports and/or cross-connect points, earthing of outer conductor or screen and coding rules.

Source

ITU-T Recommendation G.703 was prepared by ITU-T Study Group 15 (2001-2004) and approved under the WTSA Resolution 1 procedure on 29 November 2001.

History

Issue	Notes
10/2001	This revision contains the following modifications: – Addition of clause 16 on 51 840 kbit/s (STM-0) interface. – Addition of Appendix III on 3152 kbit/s interface (from G.931/Annex A). – Amendments to clause 13 on 2048 kbit/s synchronization interface. – Amendments of clauses 4, 9, 10, 11 with the inclusion of output return loss requirements for the 64 kbit/s (codirectional), 2048, 8448, 34 368 kbit/s interfaces. – Insertion of names of hierarchical interfaces (E0, E11, E21 etc.) into the headings of the corresponding clauses. – Giving of references to ITU-T Rec. G.824 (2000) with jitter parameters for the 1544 kbit/s hierarchy. Some editorial corrections were made including changes of references to the last versions of G.823, G.825 (2000).
10/98	This revision includes a correction to the specification of the 1544 and 44 736 kbit/s interfaces and the addition of Appendix I. Appendix I contains a previous version of the 1544 kbit/s interface specification. The overvoltage protection requirements have been deleted and replaced with a reference to Recommendation K.41 "Resistibility of internal interfaces of telecommunication centres to surge overvoltages". The grounding requirements for the screen (if existing) of a symmetrical pair, or the outer conductor of a coaxial cable have been enhanced. Editorial modifications are included to comply with Recommendation A.3. Clauses 1 to 12 in the 1991 revision are as a consequence renumbered into clauses 4 to 15. Appendix II on 64 and 6312 synchronization interfaces for use in Japan has been added.
1991	Previous revision
1972	Initial version

FOREWORD

The International Telecommunication Union (ITU) is the United Nations specialized agency in the field of telecommunications. The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of ITU. ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

The approval of ITU-T Recommendations is covered by the procedure laid down in WTSA Resolution 1.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

INTELLECTUAL PROPERTY RIGHTS

ITU draws attention to the possibility that the practice or implementation of this Recommendation may involve the use of a claimed Intellectual Property Right. ITU takes no position concerning the evidence, validity or applicability of claimed Intellectual Property Rights, whether asserted by ITU members or others outside of the Recommendation development process.

As of the date of approval of this Recommendation, ITU had not received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementors are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database.

CONTENTS

ITU-T Recommendation G.703

Physical/electrical characteristics of hierarchical digital interfaces

1 Scope

This Recommendation provides the recommended physical and electrical characteristics of the interfaces at hierarchical bit rates as described in ITU-T Recs. G.702 (PDH) and G.707 (SDH), to enable the interconnection of digital network components (digital sections, multiplex equipment, exchanges) to form an international digital link or connection. The characteristics given in this Recommendation should be applied to new equipment (component) designs.

NOTE 1 – The characteristics of interfaces at non-hierarchical bit rates, except $n \times 64$ kbit/s interfaces conveyed by 1544 kbit/s or 2048 kbit/s interfaces and 3152 kbit/s interface in North American hierarchy, are specified in the respective equipment Recommendations.

NOTE 2 – The jitter specifications contained in this Recommendation are intended to be imposed at international interconnection points.

NOTE 3 – The interfaces described in clauses 5 to 12 correspond to the ports T (output port) and T' (input port) as recommended for interconnection in ITU-R Rec. F.596-1 (Interconnection of digital radio-relay systems).

NOTE 4 – For signals with bit rates of $n \times 64$ kbit/s (n = 2 to 31) which are routed through multiplexing equipment specified for the 2048 kbit/s hierarchy, the interface shall have the same physical/electrical characteristics as those for the 2048 kbit/s interface specified in clause 9. For signals with bit rates of $n \times 64$ kbit/s (n = 2 to 23) which are routed through multiplexing equipment specified for the 1544 kbit/s hierarchy, the interface shall have the same physical/electrical characteristics as those for the 1544 kbit/s interface specified in clause 5.

NOTE 5 – The specifications contained in this Recommendation are related to the physical interface only (i.e. to characterize the line codes and input/output equipment interfaces); in particular, the required frequency tolerances do not imply overall equipment performances which may be driven by tighter requirements in Recommendations for specific network/equipment applications (e.g. ITU-T Recs. G.813 and G.783).

2 References

The following ITU-T Recommendations and other references contain provisions which, through reference in this text, constitute provisions of this Recommendation. At the time of publication, the editions indicated were valid. All Recommendations and other references are subject to revision; all users of this Recommendation are therefore encouraged to investigate the possibility of applying the most recent edition of the Recommendations and other references listed below. A list of the currently valid ITU-T Recommendations is regularly published.

- ITU-T Recommendation G.701 (1993), *Vocabulary of digital transmission and multiplexing, and pulse code modulation (PCM) terms.*
- ITU-T Recommendation G.702 (1988), *Digital hierarchy bit rates.*
- ITU-T Recommendation G.704 (1998), *Synchronous frame structures used at 1544, 6312, 2048, 8448 and 44 736 kbit/s hierarchical levels.*
- ITU-T Recommendation G.707/Y.1322 (2000), *Network node interface for the synchronous digital hierarchy (SDH).*
- ITU-T Recommendation G.742 (1988), *Second order digital multiplex equipment operating at 8448 kbit/s and using positive justification.*

- ITU-T Recommendation G.747 (1988), *Second order digital multiplex equipment operating at 6312 kbit/s and multiplexing three tributaries at 2048 kbit/s.*
- ITU-T Recommendation G.751 (1988), *Digital multiplex equipments operating at the third order bit rate of 34 368 kbit/s and the fourth order bit rate of 139 264 kbit/s and using positive justification.*
- ITU-T Recommendation G.752 (1988), *Characteristics of digital multiplex equipment based on a second order bit rate of 6312 kbit/s and using positive justification.*
- ITU-T Recommendation G.753 (1988), *Third order digital multiplex equipment operating at 34 368 kbit/s and using positive/zero/ negative justification.*
- ITU-T Recommendation G.755 (1988), *Digital multiplex equipment operating at 139 264 kbit/s and multiplexing three tributaries at 44 736 kbit/s.*
- ITU-T Recommendation G.811 (1997), *Timing characteristics of primary reference clocks.*
- ITU-T Recommendation G.812 (1998), *Timing requirements of slave clocks suitable for use as node clocks in synchronization networks.*
- ITU-T Recommendation G.813 (1996), *Timing characteristics of SDH equipment slave clocks (SEC).*
- ITU-T Recommendation G.823 (2000), *The control of jitter and wander within digital networks which are based on the 2048 kbit/s hierarchy.*
- ITU-T Recommendation G.824 (2000), *The control of jitter and wander within digital networks which are based on the 1544 kbit/s hierarchy.*
- ITU-T Recommendation G.825 (2000), *The control of jitter and wander within digital networks which are based on the synchronous digital hierarchy (SDH).*
- ITU-T Recommendation K.27 (1996), *Bonding configurations and earthing inside a telecommunication building.*
- ITU-T Recommendation K.41 (1998), *Resistibility of internal interfaces of telecommunication centres to surge overvoltages.*
- ITU-T Recommendation O.151 (1992), *Error performance measuring equipment operating at the primary rate and above.*
- ITU-T Recommendation O.172 (2001), *Jitter and wander measuring equipment for digital systems which are based on the synchronous digital hierarchy (SDH).*
- CCITT Handbook (1976), *Earthing of Telecommunication Installations.*
- ITU-R Recommendation F.750-3 (2000), *Architectures and functional aspects of radio-relay systems for synchronous digital hierarchy (SDH)-based networks.*
- IEC 60469-2 (1987), *Pulse techniques and apparatus. Part 2: Pulse measurement and analysis, general considerations.*
- ETSI ETS 300 166 (1993), *Transmission and Multiplexing (TM); Physical and electrical characteristics of hierarchical digital interfaces for equipment using the 2048 kbit/s-based plesiochronous or synchronous digital hierarchies.*

3 Abbreviations

This Recommendation uses the following abbreviations:

AIS Alarm Indication Signal

AMI Alternate Mark Inversion

B3ZS	Bipolar with three-Zero Substitution
B8ZS	Bipolar with eight-Zero Substitution
CMI	Coded Mark Inversion
DC	Direct Current
DSN	Digital Switching Network
EMC	Electromagnetic Compatibility
HDB2	High Density Bipolar of order 2 code
HDB3	High Density Bipolar of order 3 code
PCM	Pulse Code Modulation
PRBS	Pseudo Random Bit Sequence
PDH	Plesiochronous Digital Hierarchy
SDH	Synchronous Digital Hierarchy
STM	Synchronous Transport Module
ZBTSI	Zero Byte Time Slot Interchange

4 Interface at 64 kbit/s (E0)

4.1 Functional requirements

The following basic requirements for the design of the interface are recommended:

In both directions of transmission, three signals can be carried across the interface:

- 64 kbit/s information signal;
- 64 kHz timing signal;
- 8 kHz timing signal.

NOTE 1 – The 64 kbit/s information signal and the 64 kHz timing signal are mandatory. However, although an 8 kHz timing must be generated by the controlling equipment (e.g. PCM multiplex or time slot access equipment), it should not be mandatory for the subordinate equipment on the other side of the interface to either utilize the 8 kHz timing signal from the controlling equipment or to supply an 8 kHz timing signal.

NOTE 2 – The detection of an upstream fault can be transmitted across the 64 kbit/s interface by transmitting an alarm indication signal (AIS) towards the subordinate equipment.

The interface should be bit sequence independent at 64 kbit/s.

NOTE 3 – An unrestricted 64 kbit/s signal can be transmitted across the interface. However, this does not imply that unrestricted 64 kbit/s paths are realizable on a global basis. This is because some Administrations presently have or are continuing to install extensive networks composed of digital line sections whose characteristics do not permit the transmission of long sequences of 0s. (ITU-T Rec. G.733 provides for PCM multiplexes with characteristics appropriate for such digital line sections.) Specifically, for octet timed sources in 1544 kbit/s digital networks, it is required that at least one binary 1 should be contained in any octet of a 64 kbit/s digital signal. For a bit stream which is not octet-timed, no more than 7 consecutive 0s should appear in the 64 kbit/s signal.

NOTE 4 – Although the interface is bit sequence independent, the use of the AIS (all 1s bit pattern) may result in some minor restrictions for the 64 kbit/s source. For example, an all 1s alignment signal could result in problems.

4.1.1 Three types of envisaged interfaces

4.1.1.1 Codirectional interface

The term "codirectional" is used to describe an interface across which the information and its associated timing signal are transmitted in the same direction (see Figure 1).

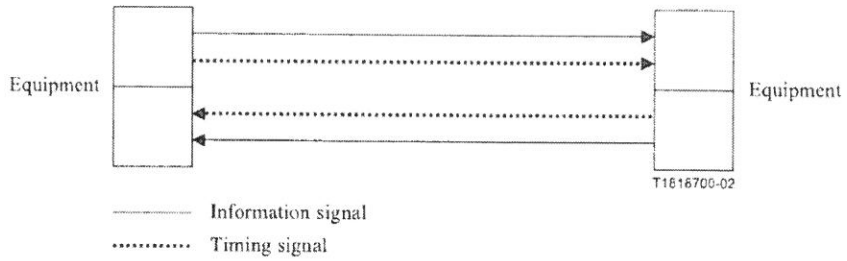


Figure 1/G.703 – Codirectional interface

4.1.1.2 Centralized clock interface

The term "centralized clock" is used to describe an interface wherein for both directions of transmission of the information signal, the associated timing signals are supplied from a centralized clock, which may be derived for example from certain incoming line signals (see Figure 2).

NOTE – The codirectional interface or centralized clock interface should be used for synchronized networks and for plesiochronous networks having clocks of the stability required (see ITU-T Rec. G.811) to ensure an adequate interval between the occurrence of slips.

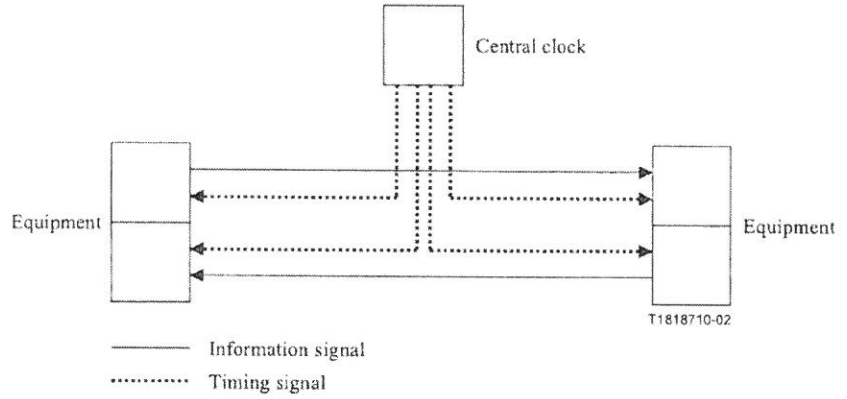


Figure 2/G.703 – Centralized clock interface

4.1.1.3 Contradirectional interface

The term "contradirectional" is used to describe an interface across which the timing signals associated with both directions of transmission are directed towards the subordinate equipment (see Figure 3).

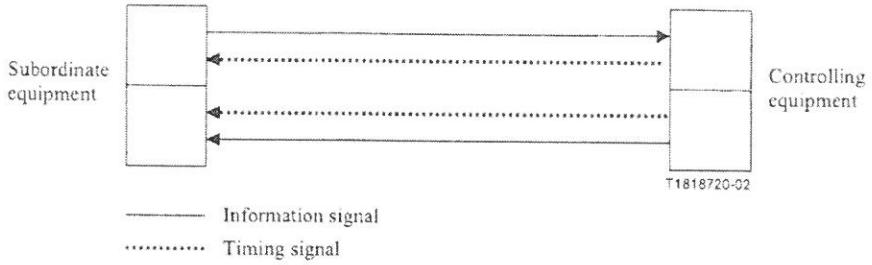


Figure 3/G.703 – Contradirectional interface

4.2 Electrical characteristics

4.2.1 Electrical characteristics of 64 kbit/s codirectional interface

4.2.1.1 General characteristics

Nominal bit rate: 64 kbit/s.

Bit rate accuracy: ±100 ppm (±6.4 bit/s) or better.

64 kHz and 8 kHz timing signal to be transmitted in a codirectional way with the information signal.

One balanced pair for each direction of transmission; the use of transformers is recommended.

Code conversion rules:

Step 1 – A 64 kbit/s bit period is divided into four unit intervals.

Step 2 – A binary one is coded as a block of the following four bits:

1 1 0 0

Step 3 – A binary zero is coded as a block of the following four bits:

1 0 1 0

Step 4 – The binary signal is converted into a three-level signal by alternating the polarity of consecutive blocks.

Step 5 – The alternation in polarity of the blocks is violated every 8th block. The violation block marks the last bit in an octet.

These conversion rules are illustrated in Figure 4.

Overvoltage protection requirements: refer to ITU-T Rec. K.41.

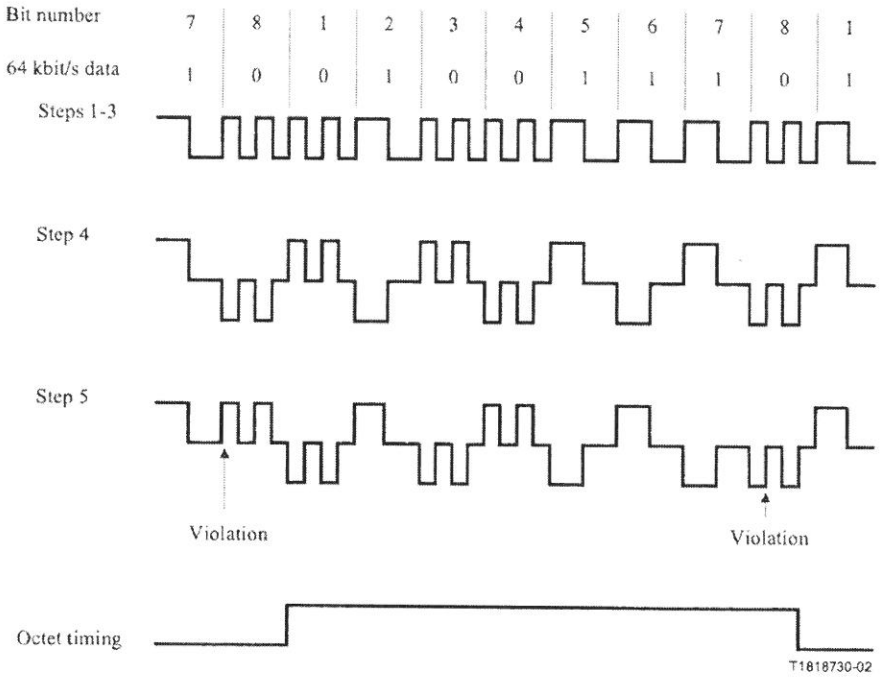


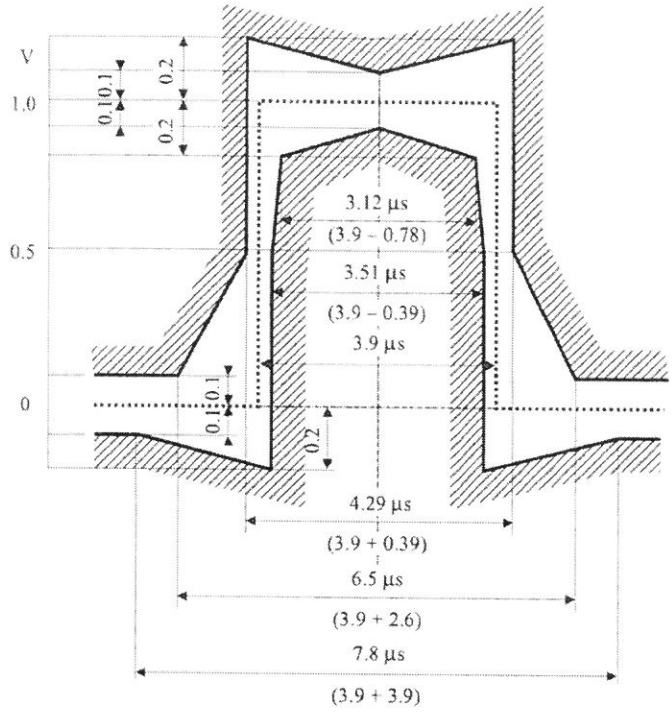
Figure 4/G.703 – Illustration of the conversion rules

4.2.1.2 Specifications at the output ports

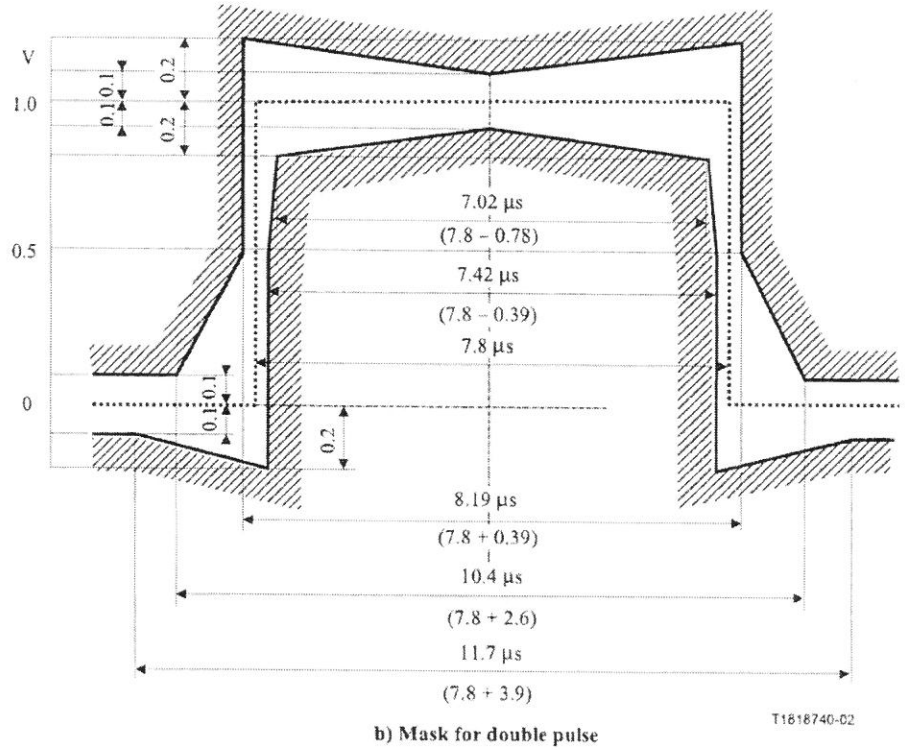
See Table 1.

Table 1/G.703 – Digital 64 kbit/s codirectional interface

Symbol rate	256 kBauds
Pulse shape (nominally rectangular)	All pulses of a valid signal must conform to the masks in Figure 5, irrespective of the polarity
Pair for each direction	One symmetric pair
Test load impedance	120 ohms resistive
Nominal peak voltage of a "mark" (pulse)	1.0 V
Peak voltage of a "space" (no pulse)	0 V ± 0.10 V
Nominal pulse width	3.9 µs
Ratio of the amplitudes of positive and negative pulses at the centre of the pulses interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05
Maximum peak-to-peak jitter at the output port (Note)	Refer to 5.1/G.823
NOTE – For the time being these values are valid only for equipments of the 2 Mbit/s hierarchy.	



a) Mask for single pulse



b) Mask for double pulse

NOTE – The limits apply to pulses of either polarity.

Figure 5/G.703 – Pulse masks of the 64 kbit/s codirectional interface

The return loss at the output port should have the following minimum values:

Frequency range (kHz)	Return loss (dB)
6.4 to 13	6
13 to 384	8

4.2.1.3 Specifications at the input ports

The digital signal presented at the input port shall be as defined above but modified by the characteristics of the interconnecting pairs. The attenuation of these pairs at a frequency of 128 kHz should be in the range 0 to 3 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

For the jitter to be tolerated at the input port, refer to 7.1.1/G.823.

The return loss at the input ports should have the following minimum values:

Frequency range (kHz)	Return loss (dB)
4 to 13	12
13 to 256	18
256 to 384	14

To provide nominal immunity against interference, input ports are required to meet the following requirements:

A nominal aggregate signal, encoded as a 64 kbit/s codirectional signal and having a pulse shape as defined in the pulse mask, shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 120 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with ITU-T Rec. O.152 (2^{11} – 1 bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

4.2.1.4 Grounding of screen

If the symmetrical pair is screened, the screen shall be connected to the bonding network both at the input port and output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult ITU-T Rec. K.27 for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

4.2.2 Electrical characteristics of the 64 kbit/s centralized clock interface

4.2.2.1 General characteristics

Nominal bit rate: 64 kbit/s. The tolerance is determined by the network clock stability (see ITU-T Rec. G.811).

For each direction of transmission, there should be one symmetrical pair carrying the data signal. In addition, there should be symmetrical pairs carrying the composite timing signal (64 kHz and

8 kHz) from the central clock source to the office terminal equipment. The use of transformers is recommended.

Overvoltage protection requirements: refer to ITU-T Rec. K.41.

Code conversion rules:

The data signals are coded in AMI code with a 100% duty ratio. The composite timing signals convey the 64 kHz bit-timing information using AMI code with a 50% to 70% duty ratio and the 8 kHz octet-phase information by introducing violations of the code rule. The structure of the signals and their nominal phase relationships are shown in Figure 6.

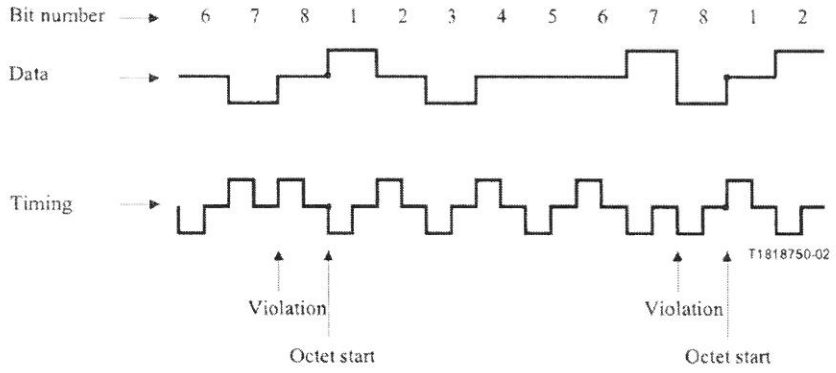


Figure 6/G.703 – Signal structures of the 64-kbit/s central clock interface at office terminal output ports

The data stream at the output ports should be timed by the leading edge of the timing pulse and the detection instant at the input ports should be timed by the trailing edge of each timing pulse.

4.2.2.2 Characteristics at the output ports

See Table 2.

Table 2/G.703 – Digital 64 kbit/s centralized clock interface

Parameters	Data	Timing
Pulse shape	Nominally rectangular, with rise and fall times less than 1 µs	Nominally rectangular, with rise and fall times less than 1 µs
Nominal test load impedance	110 ohms resistive	110 ohms resistive
Peak voltage of a "mark" (pulse) (Note 1)	a) 1.0 ± 0.1 V b) 3.4 ± 0.5 V	a) 1.0 ± 0.1 V b) 3.0 ± 0.5 V
Peak value of a "space" (no pulse) (Note 1)	a) 0 ± 0.1 V b) 0 ± 0.5 V	a) 0 ± 0.1 V b) 0 ± 0.5 V
Nominal pulse width (Note 1)	a) 15.6 µs b) 15.6 µs	a) 7.8 µs b) 9.8 to 10.9 µs
Maximum peak-to-peak jitter at the output port (Note 2)	Refer to 5.1/G.823	
NOTE 1 – The choice between the set of parameters a) and b) allows for different office noise environments and different maximum cable lengths between the three involved office equipments. NOTE 2 – For the time being, these values are valid only for equipments of the 2 Mbit/s hierarchy.		

4.2.2.3 Characteristics at the input ports

The digital signals presented at the input ports should be as defined above but modified by the characteristics of the interconnecting pairs. The varying parameters in Table 2 will allow typical maximum interconnecting distances of 350 to 450 m.

4.2.2.4 Cable characteristics

The transmission characteristics of the cable to be used are subject to further study.

4.2.3 Electrical characteristics of 64 kbit/s contradirectional interface

4.2.3.1 General characteristics

Nominal bit rate: 64 kbit/s.

Bit rate accuracy: ±100 ppm (±6.4 bit/s) or better.

For each direction of transmission there should be two symmetrical pairs of wires, one pair carrying the data signal and the other carrying a composite timing signal (64 kHz and 8 kHz). The use of transformers is recommended.

NOTE – If there is a national requirement to provide a separate alarm signal across the interface, this can be done by cutting the 8 kHz timing signal for the transmission direction concerned, i.e. by inhibiting the code violations introduced in the corresponding composite timing signal (see below).

Code conversion rules:

The data signals are coded in AMI code with a 100% duty ratio. The composite timing signals convey the 64 kHz bit-timing information using AMI code with a 50% duty ratio and the 8 kHz octet-phase information by introducing violations of the code rule. The structures of the signals and their phase relationships at data output ports are shown in Figure 7.

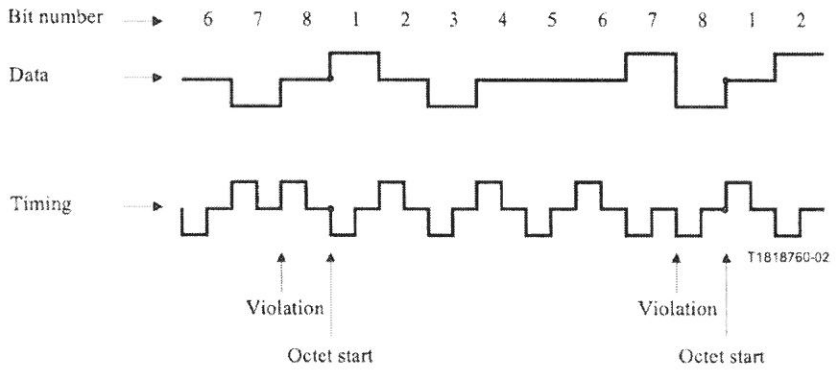


Figure 7/G.703 – Signal structures of the 64-kbit/s contradirectional interface at data output ports

The data pulses received from the service (e.g. data or signalling) side of the interface will be somewhat delayed in relation to the corresponding timing pulses. The detection instant for a received data pulse on the line side (e.g. PCM) of the interface should therefore be at the leading edge of the next timing pulse.

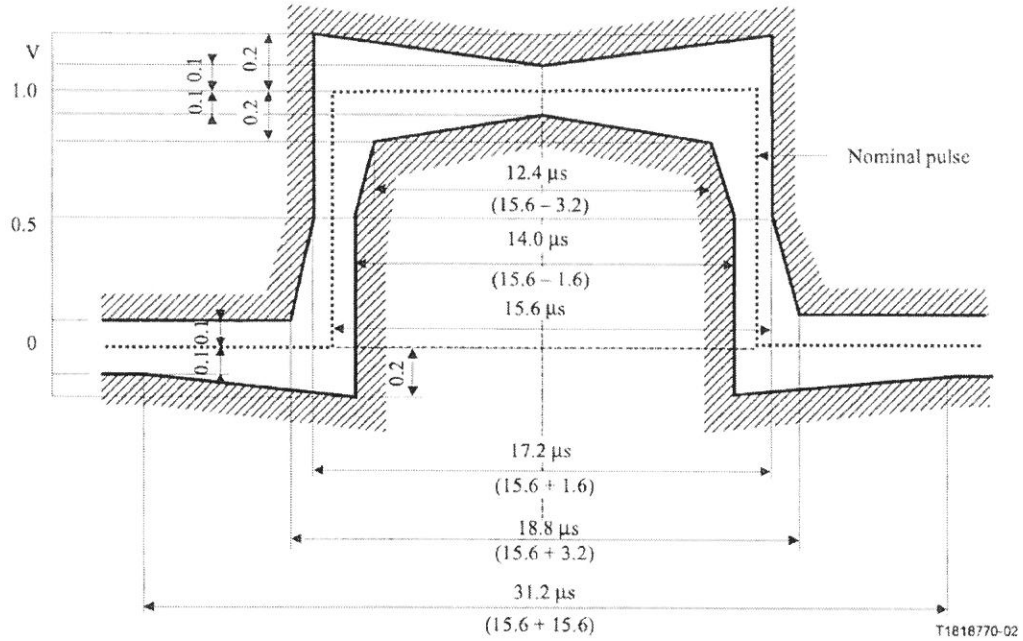
Overvoltage protection requirements: refer to ITU-T Rec. K.41.

4.2.3.2 Specifications at the output ports

See Table 3.

Table 3/G.703 – Digital 64 kbit/s contradirectional interface

Parameters	Data	Timing
Pulse shape (nominally rectangular)	All pulses of a valid signal must conform to the mask in Figure 8 irrespective of the polarity	All pulses of a valid signal must conform to the mask in Figure 9 irrespective of the polarity
Pairs in each direction of transmission	One symmetric pair	One symmetric pair
Test load impedance	120 ohms resistive	120 ohms resistive
Nominal peak voltage of a "mark" (pulse)	1.0 V	1.0 V
Peak voltage of a "space" (no pulse)	0 V ± 0.1 V	0 V ± 0.1 V
Nominal pulse width	15.6 µs	7.8 µs
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	0.95 to 1.05
Maximum peak-to-peak jitter at the output port (Note)	Refer to 5.1/G.823	
NOTE – For the time being these values are valid only for equipments of the 2 Mbit/s hierarchy.		



NOTE 1 – When one pulse is immediately followed by another pulse of the opposite polarity, the time limits at the zero-crossing between the pulses should be ±0.8 µs.

NOTE 2 – The time instants at which a transition from one state to another in the data signal may occur are determined by the timing signal. On the service (e.g. data or signalling) side of the interface, it is essential that these transitions are not initiated in advance of the timing instants given by the received timing signal.

Figure 8/G.703 – Mask of the data pulse of the 64-kbit/s contradirectional interface

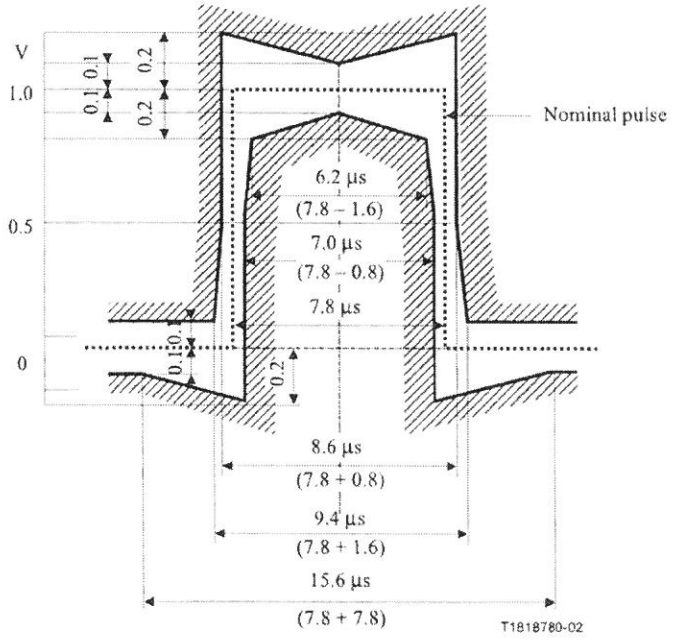


Figure 9/G.703 – Mask of the timing pulse of the 64-kbit/s contradirectional interface

4.2.3.3 Specifications at the input ports

The digital signals presented at the input ports should be as defined above but modified by the characteristics of the interconnecting pairs. The attenuation of these pairs at a frequency of 32 kHz should be in the range 0 to 3 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

The return loss at the input ports should have the following minimum values:

Frequency range (kHz)		Return loss (dB)
Data signal	Composite timing signal	
1.6 to 3.2	3.2 to 6.4	12
3.2 to 64	6.4 to 128	18
64 to 96	128 to 192	14

To provide nominal immunity against interference, input ports are required to meet the following requirement:

A nominal aggregate signal, encoded as a 64 kbit/s contradirectional signal and having a pulse shape as defined in the pulse mask, shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 120 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with ITU-T Rec. O.152 (2^{11} – 1 bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

NOTE – The return loss specification applies for both the data signal and the composite timing signal input ports.

4.2.3.4 Grounding of screen

If the symmetrical pairs are screened, the screens shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult ITU-T Rec. K.27 for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

5 Interface at 1544 kbit/s (E11)

5.1 General characteristics

The digital interface signal has a nominal bit rate of 1544 kbit/s.

The 1544 kbit/s interface specification is defined in Table 4. All signals appearing at the 1544 kbit/s interface shall satisfy each requirement listed.

Table 4/G.703 –Digital interface at 1544 kbit/s

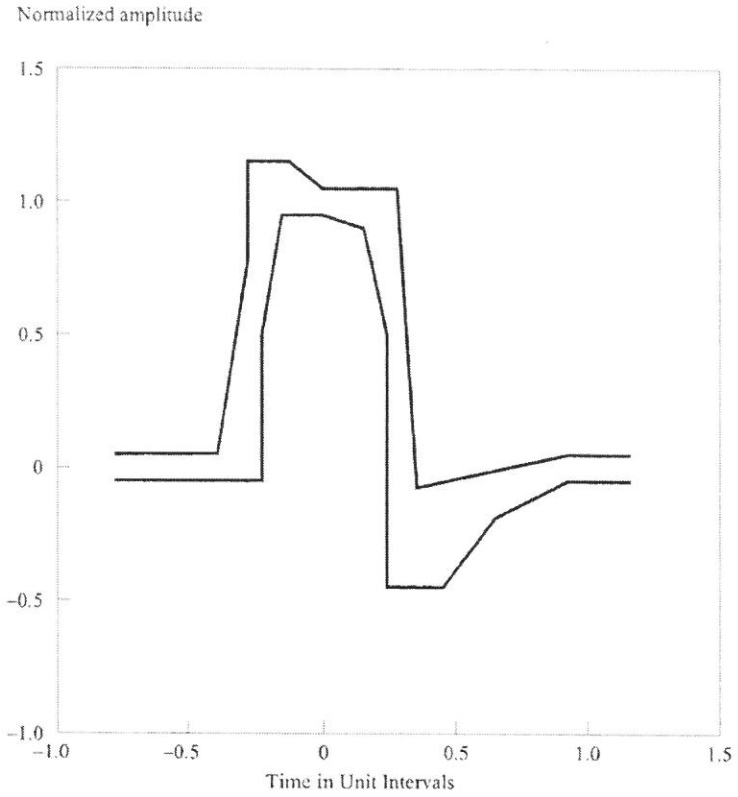
Parameter	Specification
Nominal bit rate	1544 kbit/s
Line rate accuracy	In a self-timed, free running mode, the bit rate accuracy shall be ±50 bits/s (±32 ppm) or better.
Line code	Either 1) AMI with no more than 15 consecutive zeros, and at least N ones in each and every time window of 8(N + 1) digit time slots (where N can range from 1 to 23), or 2) B8ZS (Note 1).
Frame structure	No frame structure is required for 1544 kbit/s transmission or higher level multiplexing to higher level DSN signals.
Medium	One balanced twisted pair shall be used for each direction of transmission.
Test load impedance	A resistive test load of 100 ohms ±5% shall be used at the interface for the evaluation of pulse shape and the electrical parameters specified below.
Pulse amplitude	The amplitude (Note 2) of an isolated pulse shall be between 2.4 V and 3.6 V.
Pulse shape	The shape of every pulse that approximates an isolated pulse (is preceded by four zeros and followed by one or more zeros) shall conform to the mask in Figure 10. See 5.2 for allowable procedures to be followed in checking conformance.
Power level	For an all-one signal, the power in a 3 kHz ± 1 kHz band centered at 772 kHz shall be between 12.6 dBm and 17.9 dBm. The power in a 3 kHz ± 1 kHz band centered at 1544 kHz shall be at least 29 dB below that at 772 kHz.
Pulse imbalance	In any window of seventeen consecutive bits, the maximum variation in pulse amplitudes shall be less than 200 mV, and the maximum variation in pulse widths (half amplitude) shall be less than 20 ns.
DC power	There shall be no DC power applied at the interface.
Verification access	Access to the signal at the interface shall be provided for verification of these signal specifications.
NOTE 1 – B8ZS is one method of providing bit sequence independence. Bit sequence independence in turn allows unconstrained clear channel capability. Zero Byte Time Slot Interchange (ZBTSI) is another method of providing clear channel transmission. NOTE 2 – While both voltage and power requirements are given to assist in qualification of signals at the interface, the values are not equivalent. Voltage specifications are given for isolated pulses, while power levels are specified for all-ones signal.	

Jitter requirements:

- for the maximum peak-to-peak jitter at the output port, refer to 5.1/G.824;
- for the jitter to be tolerated at the input port, refer to 7.2.1/G.824.

Overvoltage protection requirements: refer to ITU-T Rec. K.41.

An isolated pulse at the 1544 kbit/s interface shall fit within the mask shown in Figure 10. The corner points for this mask are shown below the figure. In this figure, the y axis shows normalized pulse amplitude. The x axis is time measured in unit intervals. For 1544 kbit/s, the unit interval is 648 ns.



Minimum curve		Maximum curve	
Time	Normalized amplitude	Time	Normalized amplitude
–0.77	–0.05	–0.77	0.05
–0.23	–0.05	–0.39	0.05
–0.23	0.5	–0.27	0.8
–0.15	0.95	–0.27	1.15
0.0	0.95	–0.12	1.15
0.15	0.9	0.0	1.05
0.23	0.5	0.27	1.05
0.23	–0.45	0.35	–0.07
0.46	–0.45	0.93	0.05
0.66	–0.2	1.16	0.05
0.93	–0.05		
1.16	–0.05		

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Figure 10/G.703 – 1544 kbit/s interface isolated pulse mask and corner points

Some 1544 kbit/s interface equipment embedded in the network may have been designed using a different pulse mask than that in this Recommendation. Appendix I describes the earlier specification to provide information to designers of receiving equipment on the possible range of 1544 kbit/s signals in the network.

To accommodate signals generated by equipment predating this Recommendation, the (1544 kbit/s) receivers should be capable of operation with a signal having a transmission rate of deviation of ±200 bit/s (±130 ppm) (see Appendix I for pulse characteristics of older equipment).

5.2 Pulse specification

For Alternate Mark Inversion (AMI) coding, a pulse mask describing an isolated pulse appearing at the interface is used. In most cases, an ideal isolated pulse can only be approximated due to line coding constraints.

Pulse masks are shown in normalized form, with the nominal pulse amplitude shown as 1.0. In judging conformance of an isolated pulse to the mask, it is only permissible to:

a) position the mask horizontally as needed to encompass the pulse; and

b) uniformly scale the amplitude of the isolated pulse to fit the mask.

The baseline of the signal shall coincide with the zero point of the baseline of the mask. (The determination of the signal baseline is described in IEC 60469-2). Judging the conformance of negative-going pulses shall be performed after determining the conformance of positive-going pulses in order to maintain the signal baseline reference.

When viewing inverted negative-going pulses for 1544 kbit/s, only the horizontal positioning of the mask to encompass the pulse is permitted. Note that pulse streams with any significant DC component will not meet the requirements of this clause.

5.3 Eye diagrams

For signals not amenable to the use of pulse masks, another means of specifying the quality of pulses at the interface is an eye diagram, which is formed by superimposing the waveforms of all possible pulse sequences, including the effects of intersymbol interference. Eye diagrams are presented in normalized form with the peak pulse amplitudes normalized to 1.0 on the vertical scale and the time scale shown in terms of the unit interval. In judging the shape of an eye diagram, it is permissible to:

a) position the mask horizontally as needed to encompass the eye diagram; and

b) uniformly scale the amplitude of the mask as needed to encompass the eye diagram.

The baseline of the mask shall coincide with the signal baseline. The determination of signal baseline is described in IEC 60469-2.

6 Interface at 6312 kbit/s (E21)

Interconnection of 6312 kbit/s signals for transmission purposes is accomplished at a digital distribution frame.

Nominal bit rate: 6312 kbit/s.

Bit rate accuracy: ±30 ppm (189.4 bit/s) or better.

A pseudo-ternary code shall be used as indicated in Table 5.

The shape for an isolated pulse measured at the distribution frame shall fall within the mask either of Figure 11 or of Figure 12 and meet the other requirements of Table 5.

Table 5/G.703 – Digital interface at 6312 kbit/s (Note 1)

Parameter	Specification	
Bit rate	6312 kbit/s	
Pair(s) in each direction of transmission	One symmetric pair	One coaxial pair
Code	B6ZS (Note 2)	B8ZS (Note 2)
Test load impedance	110 ohms ± 5% resistive	75 ohms ± 5% resistive
Nominal pulse shape (Note 1)	Rectangular, shaped by cable loss (see Figure 11)	Rectangular (see Figure 12)
Signal level	For an all 1s pattern transmitted, the power measured in a 3 kHz bandwidth should be as follows:	
	3156 kHz: 0.2 to 7.3 dBm 6312 kHz: –20 dBm or less	3156 kHz: 6.2 to 13.3 dBm 6312 kHz: –14 dBm or less
NOTE 1 – The pulse mask for 2nd order digital interface is shown in Figures 11 and 12. NOTE 2 – See Annex A.		

The voltage within a time slot containing a zero (space) shall be no greater than either the value produced in that time slot by other pulses (marks) within the mask of Figure 11, or ±0.1 of the peak pulse (mark) amplitude, whichever is greater in magnitude.

Jitter requirements:

- for the maximum peak-to-peak jitter at the output port, refer to 5.1/G.824;
- for the jitter to be tolerated at the input port, refer to 7.2.2/G.824.

Overvoltage protection requirements: refer to ITU-T Rec. K.41.

	T	Value of curve
Lower curve	$T \leq 0.41$	0
	$-0.41 \leq T \leq 0.24$	$0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.205}\right)\right]$
	$0.24 \leq T$	$0.331e^{-1.9(T-0.3)}$
Upper curve	$T \leq 0.72$	0
	$-0.72 \leq T \leq 0.2$	$0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.36}\right)\right]$
	$0.2 \leq T$	$0.1+0.721e^{-2.13(T-0.2)}$

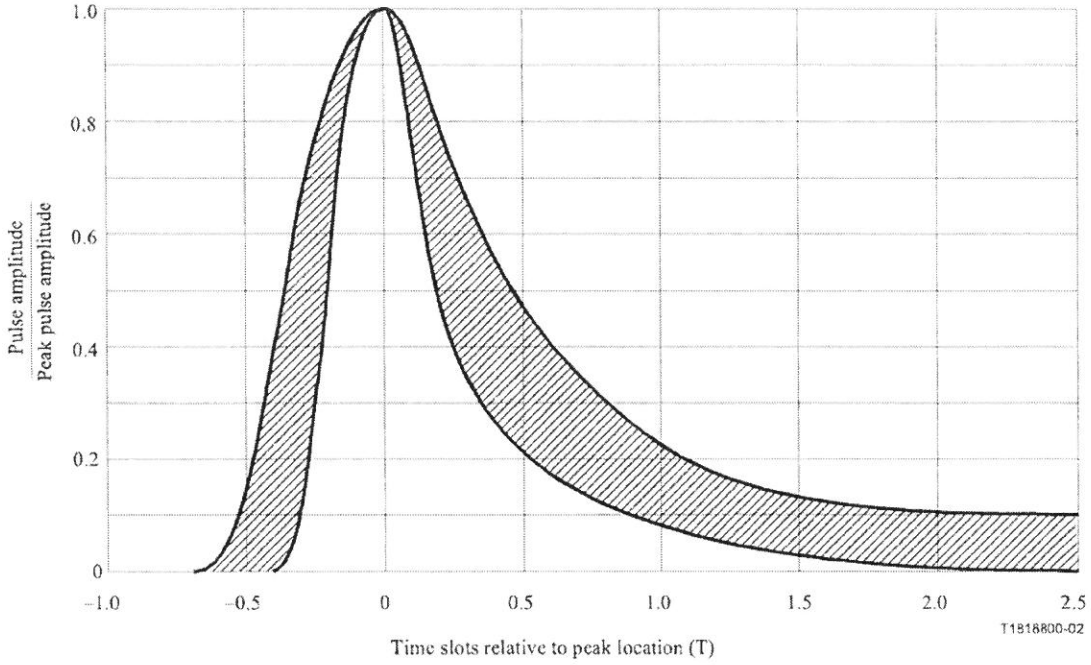


Figure 11/G.703 – Pulse mask for the symmetric pair interface at 6312 kbit/s

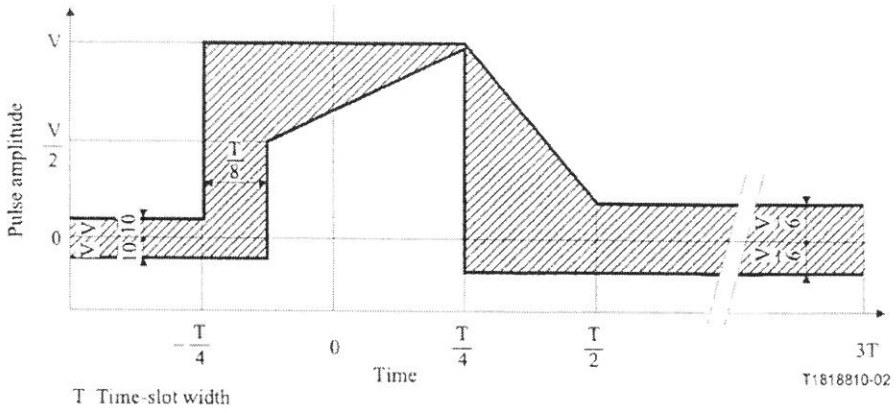


Figure 12/G.703 – Pulse mask for the coaxial pair interface at 6312 kbit/s

7 Interface at 32 064 kbit/s

Interconnection of 32 064 kbit/s signals for transmission purposes is accomplished at a digital distribution frame.

Nominal bit rate: 32 064 kbit/s.

Bit rate accuracy: ±10 ppm (±320.6 bit/s).

One coaxial pair shall be used for each direction of transmission.

The test load impedance shall be 75 ohms ± 5% resistive and the test method shall be direct.

A scrambled AMI code shall be used.

The shape for an isolated pulse measured at the point where the signal arrives at the distribution frame shall fall within the mask in Figure 13.

	T	Value of curve
Lower curve	$-0.36 \le T < -0.30$	$5.76T + 2.07$
	$-0.30 \le T < 0$	$0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.25}\right)\right]$
	$0 \le T < 0.22$	$0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.16}\right)\right]$
	$0.22 \le T$	$0.11e^{-3.42(T-0.3)}$
Upper curve	$-0.65 \le T < 0$	$1.05\left[1-e^{-4.6(T+0.65)}\right]$
	$0 \le T < 0.25$	$0.5\left[1+\sin\frac{\pi}{2}\left(1+\frac{T}{0.28}\right)\right]$
	$0.25 \le T$	$0.11+0.407e^{-2.1(T-0.29)}$

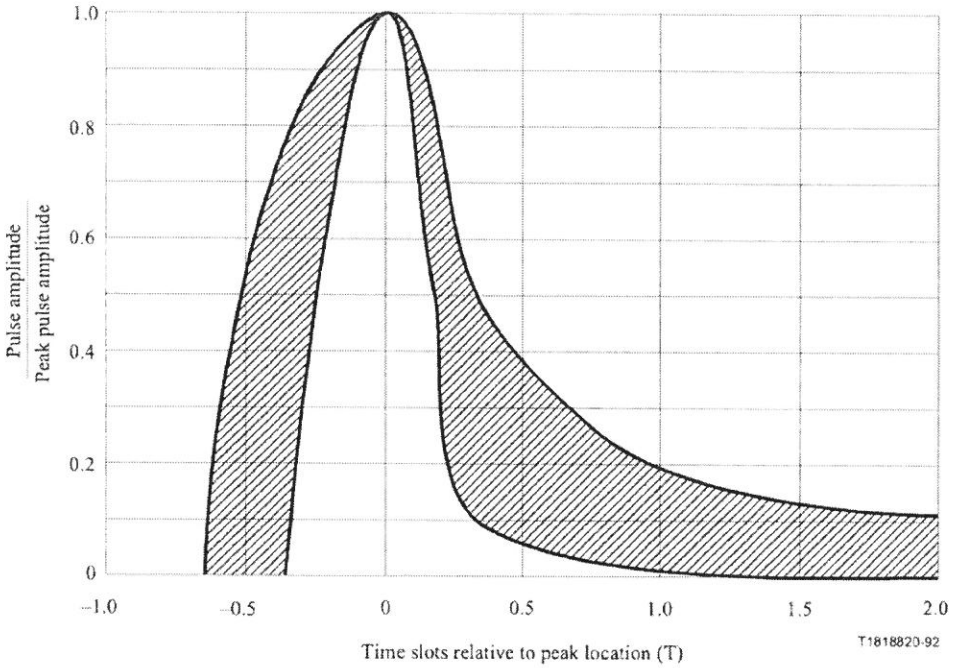


Figure 13/G.703 – Pulse mask for the coaxial pair interface at 32 064 kbit/s

The voltage within a time slot containing a zero (space) shall be no greater than either the value produced in that time slot by other pulses (marks) within the mask of Figure 13 or ±0.1 of the peak pulse (mark) amplitude, whichever is greater in magnitude.

For an all 1s pattern transmitted, the power measured in a 3 kHz bandwidth at the point where the signal arrives at the distribution frame shall be as follows:

- 16 032 kHz: + 5 dBm to + 12 dBm;
- 32 064 kHz: at least 20 dB below the power at 16 032 kHz.

The connectors and coaxial cable pairs in the distribution frame shall be 75 ohms ± 5%.

Jitter requirements:

- for the maximum peak-to-peak jitter at the output port, refer to 5.1/G.824;
- for the jitter to be tolerated at the input port, refer to 7.2.3/G.824.

Overvoltage protection requirements: refer to ITU-T Rec. K.41.

8 Interface at 44 736 kbit/s (E32)

44 736 kbit/s interface specification is defined in Table 6.

Table 6/G.703 – Digital interface at 44 736 kbit/s

Parameter	Specification
Nominal bit rate	44 736 kbit/s
Bit rate accuracy	In a self-timed, free-running mode, the bit rate accuracy shall be ±895 bits/s (±20 ppm) or better.
Line code	B3ZS (bipolar with three-zero substitutions)
Frame structure	The signal shall have the frame structure defined in ITU-T Rec. G.752 to ensure transmission through all types of 44 736 kbit/s transport equipment. The frame structure is not required for multiplexing to higher level DSN signals.
Medium	One unbalanced coaxial line shall be used for each direction of transmission.
Test load impedance	A resistive test load of 75 ohms ± 5% shall be used at the interface for the evaluation of pulse shape and the electrical parameters specified below.
Pulse amplitude	The amplitude (Note 1) of an isolated pulse shall be between 0.36 V and 0.85 V peak.
Pulse shape	The shape of every pulse that approximates an isolated pulse (is preceded by two zeros and followed by one or more zeros) shall conform to the mask in Figure 14. See 5.2 for allowable procedures to be followed in checking conformance. This mask includes an allowance of ±3% of the peak pulse amplitude at any point on the mask relative to the pulse mask in the earlier version. Equations defining the various line segments making up the mask are listed below the figure.
Power level	A wideband power measurement of an AIS signal (as defined in ITU-T Rec. G.704) using a power level sensor with a working frequency range of 200 MHz shall be between –4.7 dBm and +3.6 dBm, including the effects of a range of connecting cable lengths between 68.6 meters (225 feet) and 137.2 meters (450 feet). A low-pass filter having a flat passband and cutoff frequency of 200 MHz shall be used. The rolloff characteristics of this filter are not important; or an alternate power level specification of the power of an all-ones signal (Note 2) is useful for some equipment qualifications. It requires that the power in a 3 kHz ± 1 kHz band centered at 22 368 kHz be between –1.8 dBm and +5.7 dBm. It further requires that the power in a 3 kHz ± 1 kHz band centered at 44 736 kHz be at least 20 dB below that at 22 368 kHz.
Pulse imbalance	1) The ratio of amplitudes of positive and negative isolated pulses shall be between 0.90 and 1.10. 2) Positive and negative isolated pulses shall both conform to the mask of Figure 14.
DC power	There shall be no DC power applied at the interface.
Verification access	Access to the signal at the interface shall be provided for verification of these signal specifications.

Parameter	Specification
NOTE 1 – While both voltage and power requirements are given to assist in qualification of signals at the interface, the values are not equivalent. Voltage specifications are given for isolated pulses, while power levels are specified for an AIS signal, or alternatively an all-ones signal. NOTE 2 – The all-ones signal is not realizable within the frame structure specified in Recommendation G.752, and is not encountered in North American telecommunication networks.	

All signals appearing at the 44 736 kbit/s interface shall satisfy each requirement listed.

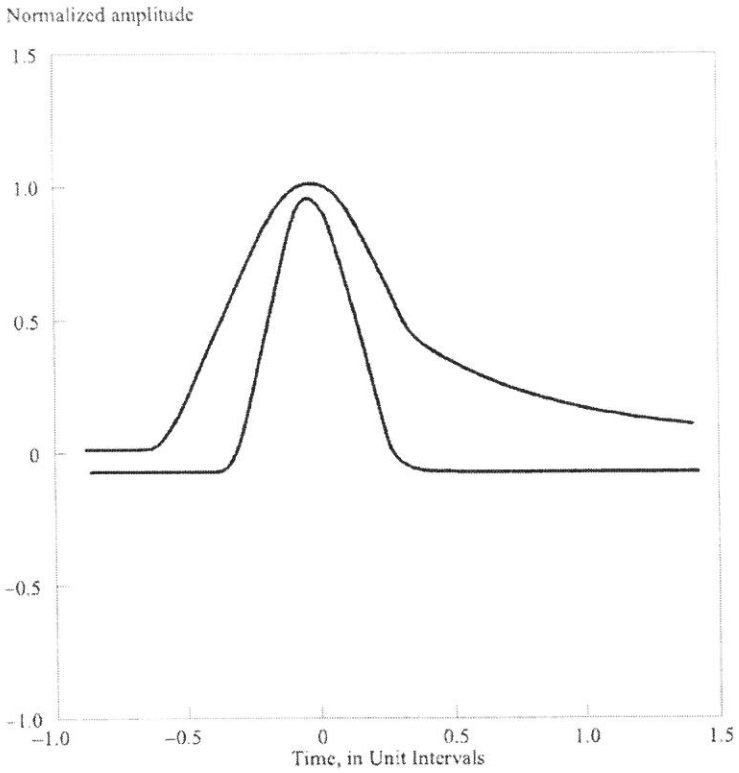
An isolated pulse (see pulse shape in Table 6) at the 44 736 kbit/s interface shall fit within the mask shown in Figure 14. Equations defining the various line segments making up the mask are listed below the figure. In this figure, the y axis shows normalized pulse amplitude. The x axis is time measured in unit intervals. For 44 736 kbit/s, the unit interval is 22.4 ns.

To assure proper operation of transmission facilities and higher order multiplex equipment, all 44 736 kbit/s sources shall use the frame structured defined in ITU-T Rec. G.752.

Jitter requirements:

- for the maximum peak-to-peak jitter at the output port, refer to 5.1/G.824;
- for the jitter to be tolerated at the input port, refer to 7.2.4/G.824.

Overvoltage protection requirements: refer to ITU-T Rec. K.41.



Time axis range (Unit Intervals)	Normalized amplitude equation
Upper curve	
$-0.85 \le T \le -0.68$	0.03
$-0.68 \le T \le 0.36$	$0.5\left\{1+\sin\left[\frac{\pi}{2}\left(1+\frac{T}{0.34}\right)\right]\right\}+0.03$
$0.36 \le T \le 1.4$	$0.08+0.407e^{-1.84(T-0.36)}$
Lower curve	
$-0.85 \le T \le -0.36$	–0.03
$-0.36 \le T \le 0.36$	$0.5\left\{1+\sin\left[\frac{\pi}{2}\left(1+\frac{T}{0.18}\right)\right]\right\}-0.03$
$0.36 \le T \le 1.4$	–0.03

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Figure 14/G.703 – 44 736 kbit/s interface isolated pulse mask and equations

9 Interface at 2048 kbit/s (E12)

9.1 General characteristics

Nominal bit rate: 2048 kbit/s.

Bit rate accuracy: ±50 ppm (±102.4 bit/s).

Code: High density bipolar of order 3 (HDB3) (a description of this code can be found in Annex A).

Overvoltage protection requirements: refer to ITU-T Rec. K.41.

9.2 Specifications at the output ports

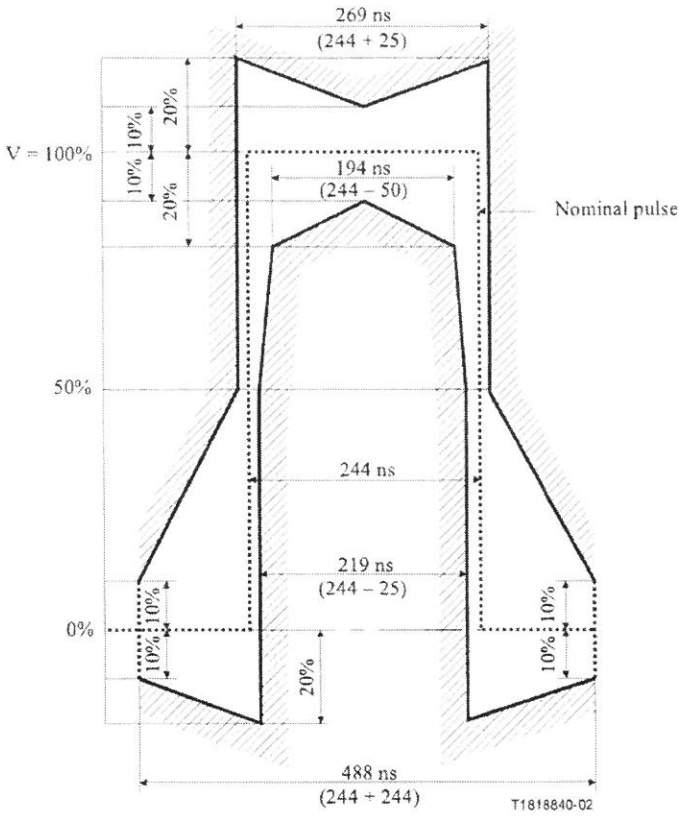
See Table 7.

Table 7/G.703 – Digital interface at 2048 kbit/s

Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (see Figure 15) irrespective of the sign. The value V corresponds to the nominal peak value.	
Pair(s) in each direction	One coaxial pair (see 9.4)	One symmetrical pair (see 9.4)
Test load impedance	75 ohms resistive	120 ohms resistive
Nominal peak voltage of a mark (pulse)	2.37 V	3 V
Peak voltage of a space (no pulse)	0 ± 0.237 V	0 ± 0.3 V
Nominal pulse width	244 ns	
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05	
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05	
Maximum peak-to-peak jitter at an output port	Refer to 5.1/G.823	

The return loss at the output port should have the following minimum values:

Frequency range (kHz)	Return loss (dB)
51 to 102	6
102 to 3072	8



NOTE – V corresponds to the nominal peak value.

Figure 15/G.703 – Mask of the pulse at the 2048 kbit/s interface

9.3 Specifications at the input ports

The digital signal presented at the input port shall be as defined above but modified by the characteristic of the interconnecting pair. The attenuation of this pair shall be assumed to follow a $\sqrt{f}$law and the loss at a frequency of 1024 kHz shall be in the range 0 to 6 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

For the jitter to be tolerated at the input port, refer to 7.1.2/G.823.

The return loss at the input port should have the following provisional minimum values:

Frequency range (kHz)	Return loss (dB)
51 to 102	12
102 to 2048	18
2048 to 3072	14

To ensure adequate immunity against signal reflections that can arise at the interface due to impedance irregularities at digital distribution frames and at digital output ports, input ports should meet the following requirement:

A nominal aggregate signal, encoded into HDB3 and having a pulse shape as defined in the pulse mask, shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 75 ohms (in the case of coaxial-pair interface) or 120 Ohms (in the case of symmetrical-pair interface), to give a signal-to-interference ratio of 18 dB. The binary content of the interfering signal should comply with ITU-T Rec. O.151 ($2^{15} - 1$ bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

NOTE – A receiver implementation providing an adaptive rather than a fixed threshold is considered to be more robust against reflections and should therefore be preferred.

9.4 Grounding of outer conductor or screen

The outer conductor of the coaxial pair or the screen of the symmetrical pair shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult ITU-T Rec. K.27 for guidance.

NOTE 2 – The direct connection of the outer conductors of coaxial cables to the bonding network at the transmit and receive interfaces may, because of differences in earth potential at each end of the cable, result in unwanted current flowing in the outer conductor, through connectors and through the receiver input circuitry. This may result in errors or even permanent damage. To prevent this problem, DC isolation may be introduced between the outer conductor and bonding network at the receive interface. The method of DC isolation must not compromise the EMC compliance of the equipment and the overall installation.

NOTE 3 – The use of isolation to the bonding network is for further study.

10 Interface at 8448 kbit/s (E22)

10.1 General characteristics

Nominal bit rate: 8448 kbit/s.

Bit rate accuracy: ±30 ppm (±253.4 bit/s).

Code: High density bipolar of order 3 HDB3 (a description of this code can be found in Annex A).

Overvoltage protection requirements: refer to ITU-T Rec. K.41.

10.2 Specification at the output ports

See Table 8.

Table 8/G.703 – Digital interface at 8448 kbit/s

Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (Figure 16) irrespective of the sign.
Pair(s) in each direction	One coaxial pair (see 10.4)
Test load impedance	75 ohms resistive
Nominal peak voltage of a mark (pulse)	2.37 V
Peak voltage of a space (no pulse)	0 V ± 0.237 V
Nominal pulse width	59 ns
Ratio of the amplitudes of positive and negative pulses at the centre of the pulse interval	0.95 to 1.05
Ratio of widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05
Maximum peak-to-peak jitter at an output port	Refer to 5.1/G.823

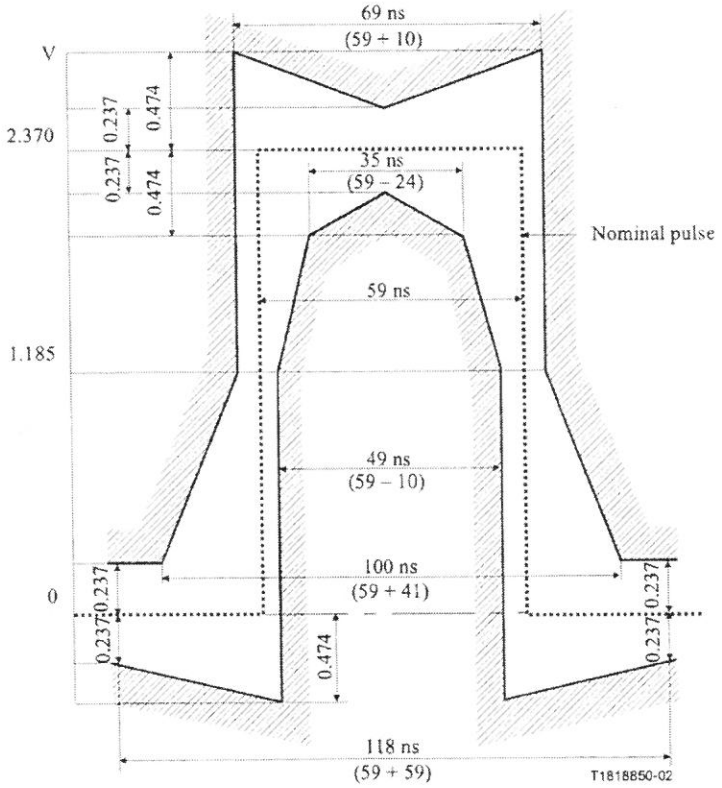


Figure 16/G.703 – Pulse mask at the 8448 kbit/s interface

The return loss at the output port should have the following minimum values:

Frequency range (kHz)	Return loss (dB)
211 to 422	6
422 to 12 672	8

10.3 Specifications at the input ports

The digital signal presented at the input port shall be as defined above but modified by the characteristics of the interconnecting pairs. The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at a frequency of 4224 kHz shall be in the range 0 to 6 dB. This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

For the jitter to be tolerated at the input port, refer to 7.1.3/G.823.

The return loss at the input port should have the following provisional minimum values:

Frequency range (kHz)	Return loss (dB)
211 to 422	12
422 to 8448	18
8448 to 12 672	14

To ensure adequate immunity against signal reflections that can arise at the interface due to impedance irregularities at digital distribution frames and at digital output ports, input ports should meet the following requirement:

A nominal aggregate signal, encoded into HDB3 and having a pulse shape as defined in the pulse mask shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within the limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 75 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with ITU-T Rec. O.151 (2^{15} – 1 bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

10.4 Grounding of outer conductor

The outer conductor of the coaxial pair shall be connected to the bonding network at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult ITU-T Rec. K.27 for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

11 Interface at 34 368 kbit/s (E31)

11.1 General characteristics

Nominal bit rate: 34 368 kbit/s.

Bit rate accuracy: ±20 ppm (±688 bit/s).

Code: HDB3 (a description of this code can be found in Annex A).

Overvoltage protection requirements: refer to ITU-T Rec. K.41.

11.2 Specification at the output ports

See Table 9.

Table 9/G.703 – Digital interface at 34 368 kbit/s

Pulse shape (nominally rectangular)	All marks of a valid signal must conform with the mask (see Figure 17), irrespective of the sign.
Pair(s) in each direction	One coaxial pair (see 11.4)
Test load impedance	75 ohms resistive
Nominal peak voltage of a mark (pulse)	1.0 V
Peak voltage of a space (no pulse)	0 V ± 0.1 V
Nominal pulse width	14.55 ns
Ratio of the amplitudes of positive and negative pulses at the center of a pulse interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05
Maximum peak-to-peak jitter at an output port	Refer to 5.1/G.823

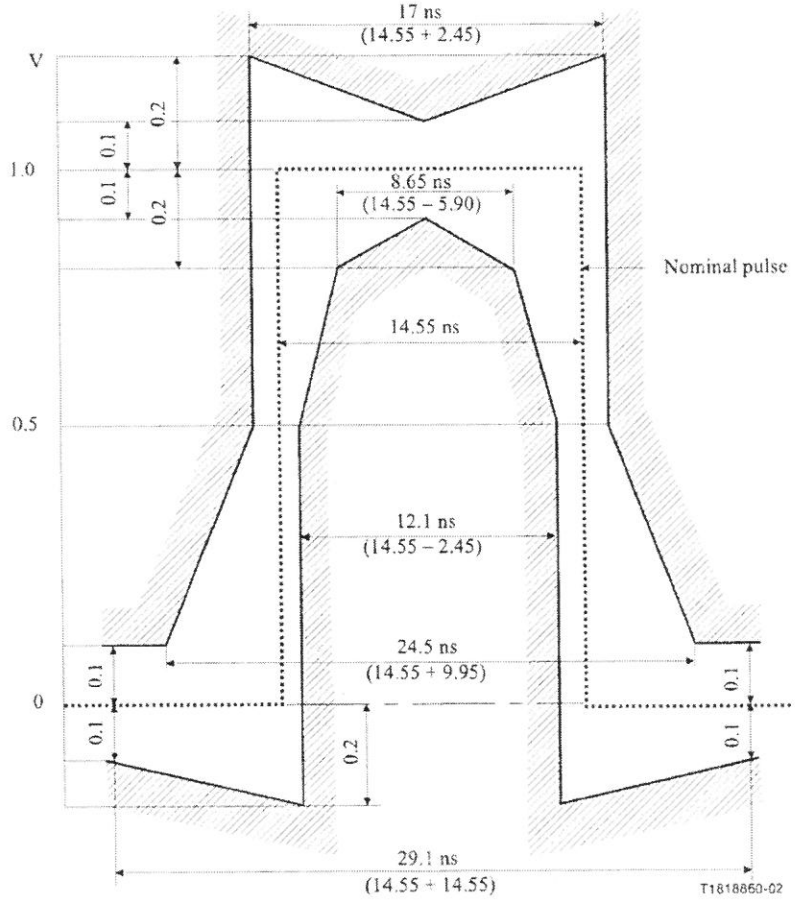


Figure 17/G.703 – Pulse mask at the 34 368 kbit/s interface

The return loss at the output port should have the following minimum values:

Frequency range (kHz)	Return loss (dB)
860 to 1720	6
1720 to 51 550	8

11.3 Specifications at the input ports

The digital signal presented at the input port shall be as defined above but modified by the characteristics of the interconnecting pair. The attenuation of this cable shall be assumed to follow approximately a $\sqrt{f}$ law and the loss at a frequency of 17 184 kHz shall be in the range 0 to 12 dB.

For the jitter to be tolerated at the input port, refer to 7.1.4/G.823.

The return loss at the input port should have the following provisional minimum values:

Frequency range (kHz)	Return loss (dB)
860 to 1720	12
1720 to 34 368	18
34 368 to 51 550	14

To ensure adequate immunity against signal reflections that can arise at the interface due to impedance irregularities at digital distribution frames and at digital output ports, input ports are required to meet the following requirement:

A nominal aggregate signal, encoded into HDB3 and having a pulse shape as defined in the pulse mask shall have added to it an interfering signal with the same pulse shape as the wanted signal. The interfering signal should have a bit rate within limits specified in this Recommendation, but should not be synchronous with the wanted signal. The interfering signal shall be combined with the wanted signal in a combining network, with an overall zero loss in the signal path and with the nominal impedance 75 ohms to give a signal-to-interference ratio of 20 dB. The binary content of the interfering signal should comply with ITU-T Rec. O.151 ($2^{23} - 1$ bit period). No errors shall result when the combined signal, attenuated by up to the maximum specified interconnecting cable loss, is applied to the input port.

11.4 Grounding of outer conductor

The outer conductor of the coaxial pair shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult ITU-T Rec. K.27 for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

12 Interface at 139 264 kbit/s (E4)

12.1 General characteristics

Nominal bit rate: 139 264 kbit/s.

Bit rate accuracy: ±15 ppm (±2089 bit/s).

Code: Coded Mark Inversion (CMI) (a description of this code can be found in Annex A)

Overvoltage protection requirements: refer to ITU-T Rec. K.41.

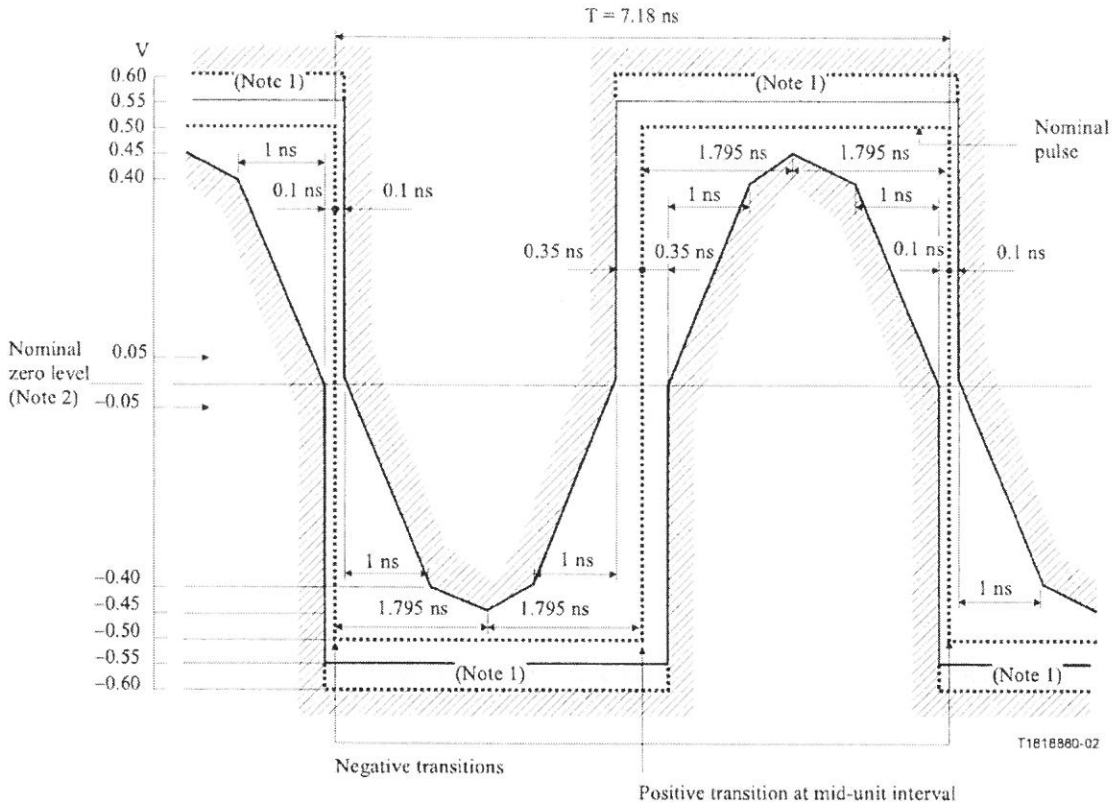
12.2 Specifications at the output ports

The specifications at the output ports are given in Table 10 and Figures 18 and 19.

NOTE – A method based on the measurement of the levels of the fundamental frequency component, the second (and possibly the third) harmonic of a signal corresponding to binary all 0s and binary all 1s, is considered to be a perfectly adequate method of checking that the requirements of Table 10 have been met. The relevant values of the harmonic components are under study.

Table 10/G.703 – Digital interface at 139 264 kbit/s

Pulse shape	Nominally rectangular and conforming to the masks shown in Figures 18 and 19
Pair(s) in each direction	One coaxial pair
Test load impedance	75 ohms resistive
Peak-to-peak voltage	1 ± 0.1 V
Rise time between 10% and 90% amplitudes of the measured steady state amplitude	≤2 ns
Transition timing tolerance (referred to the mean value of the 50% amplitude points of negative transitions)	Negative transitions: ±0.1 ns Positive transitions at unit interval boundaries: ±0.5 ns Positive transitions at mid-interval: ±0.35 ns
Return loss	≥15 dB over frequency range 7 MHz to 210 MHz
Maximum peak-to-peak jitter at an output port	Refer to 5.1/G.823



NOTE 1 – The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 µF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

NOTE 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident.

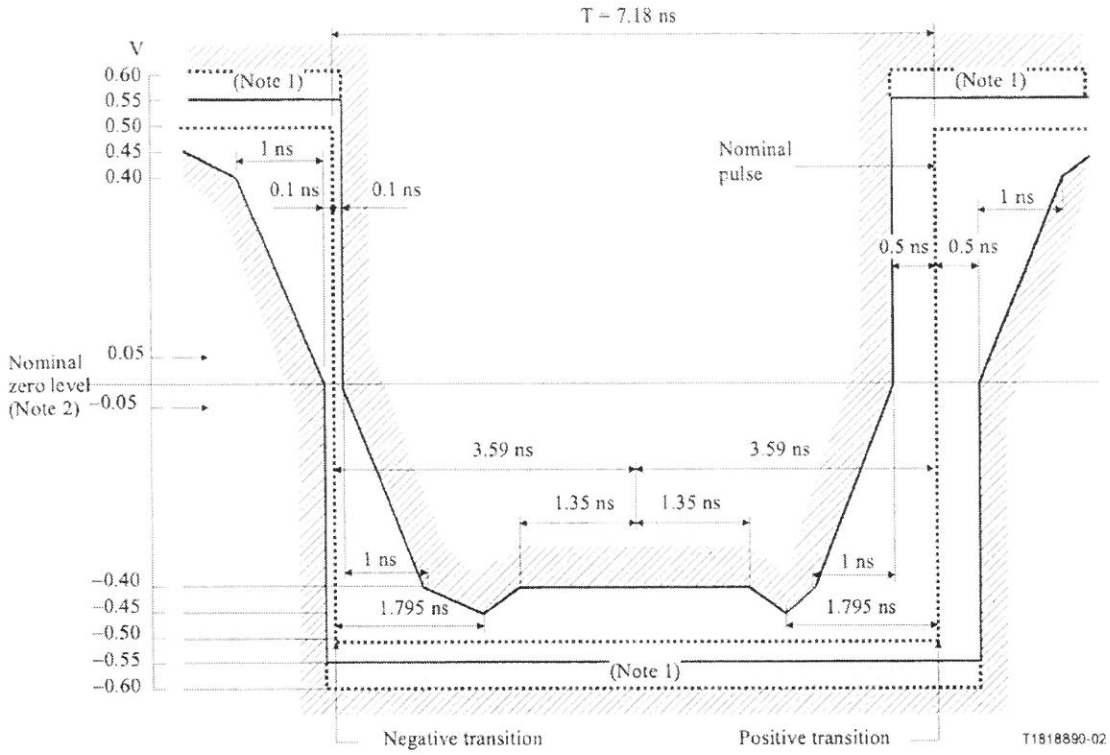
The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.

When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

These techniques require further study.

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between –0.4 V and 0.4 V, and should not exceed 2 ns.

Figure 18/G.703 – Mask of a pulse corresponding to a binary 0 at the 139 264 kbit/s interface



NOTE 1 – The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 µF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

NOTE 3 – Each pulse in a coded sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident.

The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.

When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

These techniques require further study.

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between –0.4 V and 0.4 V, and should not exceed 2 ns.

NOTE 5 – The inverse pulse will have the same characteristics, noting that the timing tolerance at the level of the negative and positive transitions are ±0.1 ns and ±0.5 ns respectively.

Figure 19/G.703 – Mask of a pulse corresponding to a binary 1 at the 139 264 kbit/s interface

12.3 Specifications at the input ports

The digital signal presented at the input port should conform to Table 10 and Figures 18 and 19 modified by the characteristics of the interconnecting coaxial pair.

The attenuation of the coaxial pair should be assumed to follow an approximate $\sqrt{f}$ law and to have a maximum insertion loss of 12 dB at a frequency of 70 MHz.

For the jitter to be tolerated at the input port, refer to 7.1.5/G.823.

The return loss characteristics should be the same as that specified for the output port.

12.4 Grounding of outer conductor

The outer conductor of the coaxial pair shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult ITU-T Rec. K.27 for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

13 2048 kHz synchronization interface (T12)

13.1 General characteristics

The use of this interface is recommended for all applications where it is required to synchronize a digital equipment by an external 2048 kHz synchronization signal.

Overvoltage protection requirements: refer to ITU-T Rec. K.41.

13.2 Specifications at the output ports

For general characteristics, see Table 11; for frequency accuracy requirements, see Table 11a.

Table 11/G.703 – Digital 2048 kHz clock interface

Pulse shape	The signal must conform with the mask (Figure 20). The value V corresponds to the maximum peak value. The value V_1 corresponds to the minimum peak value.	
Type of pair	Coaxial pair (see Note in 13.4)	Symmetrical pair (see Note in 13.4)
Test load impedance	75 ohms resistive	120 ohms resistive
Maximum peak voltage (V_{op})	1.5	1.9
Minimum peak voltage (V_{op})	0.75	1.0
Maximum jitter at an output port	Refer to Table 5/G.823 (Note)	
NOTE – This value is valid for network timing synchronization equipments. Other values may be specified for timing output ports of digital links carrying the network timing.		

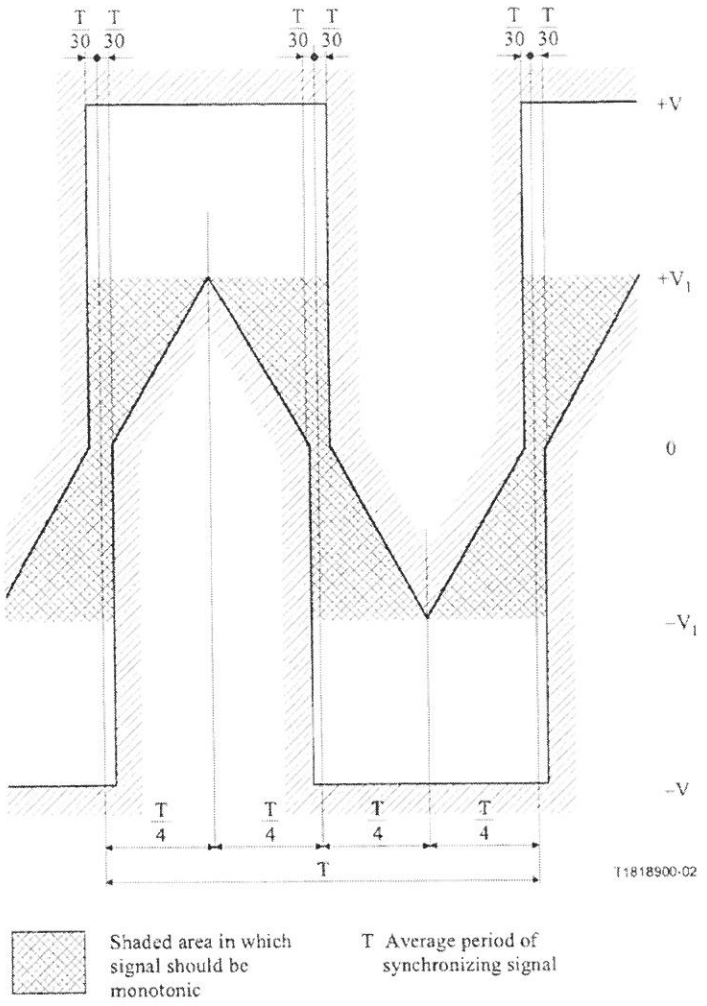


Figure 20/G.703 – Wave shape at an output port of the 2048 kHz synchronization interface

Table 11a/G.703 – Digital 2048 kHz clock – Frequency accuracy at output ports

Output interface	Required accuracy
Primary reference clock – PRC	Refer to ITU-T Rec. G.811
Synchronization supply unit – SSU	Refer to ITU-T Rec. G.812
SDH equipment clock – SEC	4.6 ppm; refer also to ITU-T Rec. G.813
Others (Note)	±50 ppm
NOTE – Synchronization interfaces defined in the 1998 version of this Recommendation.	

13.3 Specifications at the input ports

The signal presented at the input ports should be as defined above but modified by the characteristics of the interconnecting pair.

The attenuation of this pair shall be assumed to follow a $\sqrt{f}$ law and the loss at a frequency of 2048 kHz should be in the range 0 to 6 dB (minimum value). This attenuation should take into account any losses incurred by the presence of a digital distribution frame between the equipments.

The input port shall be able to tolerate a digital signal with these electrical characteristics but modulated by jitter. See Table 11b.

The return loss at 2048 kHz should be ≥15 dB.

Table 11b/G.703 – Digital 2048 kHz clock – Noise tolerance at input ports

Input interface	Jitter tolerance
Primary reference clock – PRC	Not applicable
Synchronization supply unit – SSU	Refer to ITU-T Rec. G.812
SDH equipment clock – SEC	Refer to ITU-T Rec. G.813
Others (Note)	For further study
NOTE – Synchronization interfaces defined in the 1998 version of this Recommendation.	

13.4 Grounding of outer conductor or screen

The outer conductor of the coaxial pair or the screen of the symmetrical pair shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult ITU-T Rec. K.27 for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

14 Interface at 97 728 kbit/s

Interconnection of 97 728 kbit/s signals for transmission purposes is accomplished at a digital distribution frame.

Nominal bit rate: 97 728 kbit/s.

Bit rate accuracy: ±10 ppm (±978 bit/s).

One coaxial pair shall be used for each direction of transmission.

The test load impedance shall be 75 ohms ± 5% resistive.

A scrambled AMI code[1] shall be used.

The shape for the 97 728 kbit/s output port shall fall within the mask in Figure 21. The shape at the point where the signal arrives at the distribution frame will be modified by the characteristics of the interconnecting cable.

[1] An AMI code is scrambled by a five-stage reset-type scrambler with the primitive polynomial of $x^5 + x^3 + 1$.

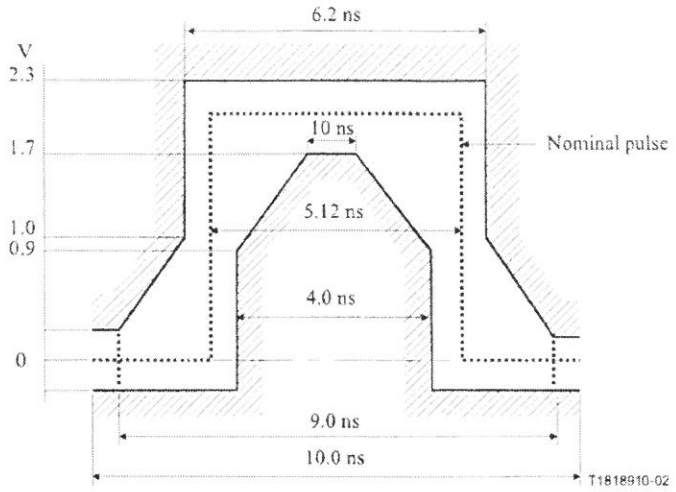


Figure 21/G.703 – Pulse mask at the 97 728 kbit/s output port

The connectors and cable pairs in the distribution frame shall be 75 ohms ± 5%.

Jitter requirements:

- for the maximum peak-to-peak jitter at the output port, refer to 5.1/G.824;
- for the jitter to be tolerated at the input port, refer to 7.2.5/G.824.

Overvoltage protection requirements: refer to ITU-T Rec. K.41.

15 Interface at 155 520 kbit/s – STM-1 interface (ES1)

15.1 General characteristics

Nominal bit rate: 155 520 kbit/s.

Bit rate accuracy: ±20 ppm (±3111 bit/s).

Code: Coded Mark Inversion (CMI) (a description of this code can be found in Annex A).

Overvoltage protection requirements: refer to ITU-T Rec. K.41.

15.2 Specifications at the output ports

The specifications at the output ports are given in Table 12 and in Figures 22 and 23.

NOTE – A method based on the measurement of the levels of the fundamental frequency component, the second (and possibly the third) harmonic of a signal corresponding to the binary all 0s and binary all 1s, is considered to be a perfectly adequate method of checking that the requirements of Table 12 have been met. The relevant values of the harmonic components are under study.

Table 12/G.703 – Digital interface at 155 520 kbit/s

Pulse shape	Nominally rectangular and conforming to the masks shown in Figures 22 and 23
Pair(s) in each direction	One coaxial pair
Test load impedance	75 ohms resistive
Peak-to-peak voltage	1 ± 0.1 V
Rise time between 10% and 90% amplitudes of the measured steady state amplitude	≤2 ns
Transition timing tolerance referred to the mean value of the 50% amplitude points of negative transitions	Negative transitions: ±0.1 ns Positive transitions at unit interval boundaries: ±0.5 ns Positive transitions at mid-unit intervals: ±0.35 ns
Return loss	≥15 dB over frequency range 8 MHz to 240 MHz
Maximum peak-to-peak jitter at an output port	Refer to 5.1/G.825

15.3 Specifications at the input ports

The digital signal presented at the input port should conform to Table 12 and Figures 22 and 23 modified by the characteristics of the interconnecting coaxial pair.

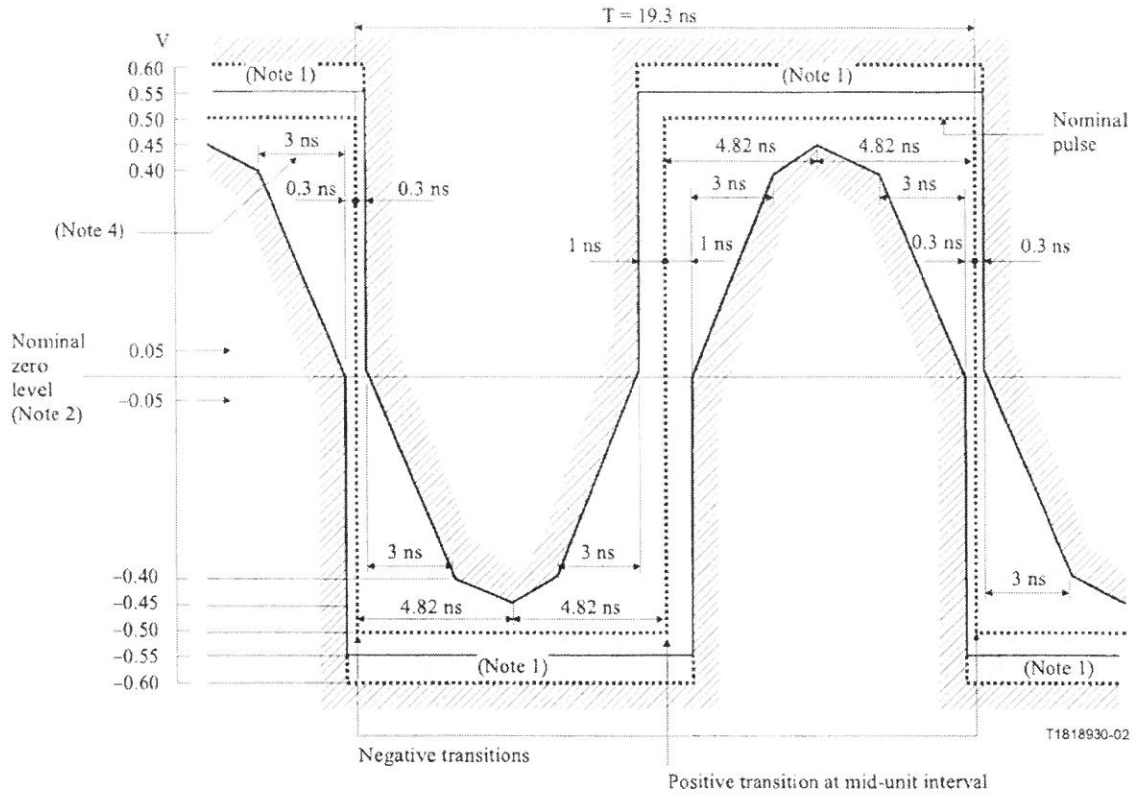
The attenuation of the coaxial pair should be assumed to follow an approximate $\sqrt{f}$ law and to have a maximum insertion loss of 12.7 dB at a frequency of 78 MHz.

For the jitter to be tolerated at the input port, refer to 6.1.2.1/G.825.

The return loss characteristics should be the same as that specified for the output port.

15.4 Specifications at the cross-connect points

- *Signal power level*: A wideband power measurement using a power level sensor with a working frequency range of at least 300 MHz shall be between –2.5 and +4.3 dBm. There shall be no DC power transmitted across the interface.
- *Eye diagram*: An eye diagram mask based on the maximum and minimum power levels given above is shown in Figure 24 where the voltage amplitude has been normalized to one, and the time scale is specified in terms of the pulse repetition period T. The corner points of the eye diagram are shown in Figure 24.
- *Termination*: One coaxial cable shall be used for each direction of transmission.
- *Impedance*: A resistive test load of 75 ohms ±5% shall be used at the interface for the evaluation of the eye diagram and the electrical parameters of the signal.



NOTE 1 – The maximum "steady state" amplitude should not exceed the 0.55 Vlimit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 µF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

NOTE 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident.

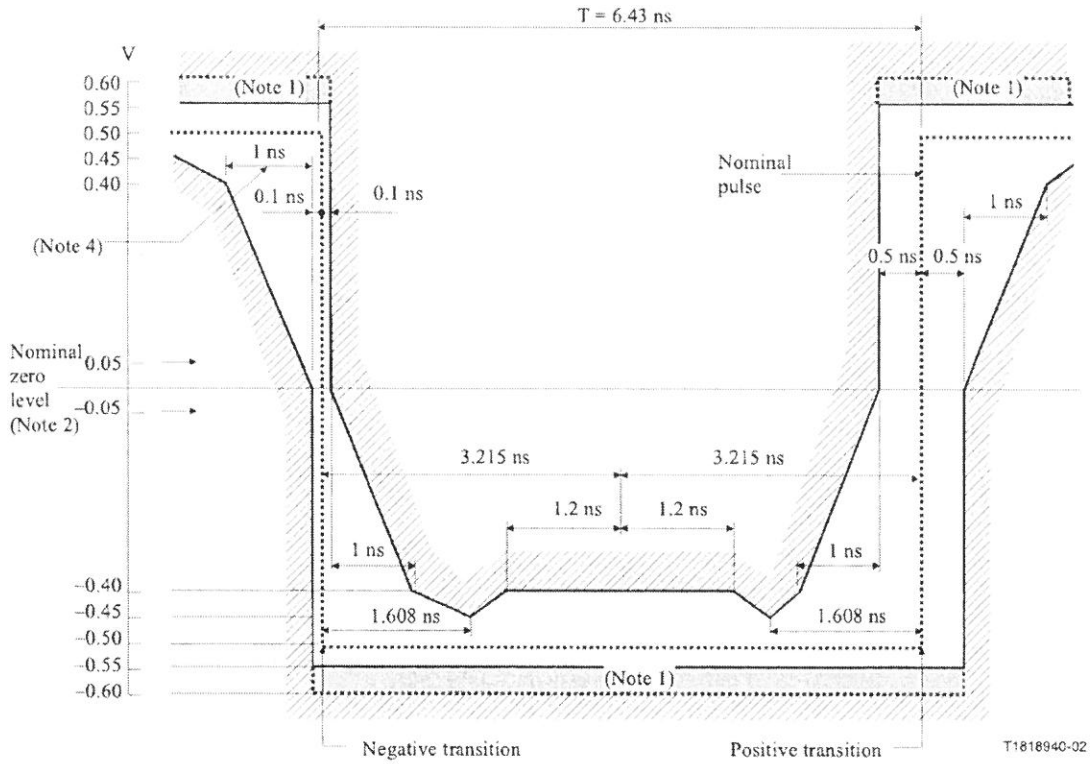
The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.

When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

These techniques require further study.

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between –0.4 V and 0.4 V, and should not exceed 2 ns.

Figure 22/G.703 – Mask of a pulse corresponding to a binary 0 (at the 155 520 kbit/s interface)



NOTE 1 – The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 μF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

NOTE 3 – Each pulse in a coded sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident.

The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.

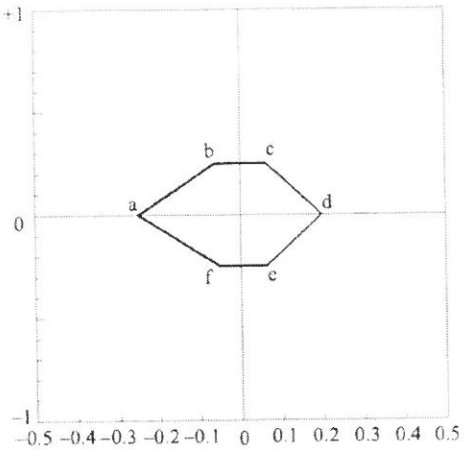
When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of thepulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

These techniques require further study.

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between –0.4 V and 0.4 V, and should not exceed 2 ns.

NOTE 5 – The inverse pulse will have the same characteristics, noting that the timing tolerance at the level of the negative and positive transitions are ±0.1 ns and ±0.5 ns respectively.

Figure 23/G.703 – Mask of a pulse corresponding to a binary 1 (at the 155 520 kbit/s interface)



Point	Time	Amplitude
a	$-0.25\frac{T}{2}$	0.00
b	$-0.05\frac{T}{2}$	+0.25
c	$+0.05\frac{T}{2}$	+0.25
d	$+0.20\frac{T}{2}$	0.00
e	$+0.05\frac{T}{2}$	−0.25
f	$-0.05\frac{T}{2}$	−0.25

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Figure 24/G.703 – STM-1 interface eye diagram

15.5 Grounding of outer conductor

The outer conductor of the coaxial pair shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult ITU-T Rec. K.27 for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

16 Interface at 51 840 kbit/s (STM-0 interface)

16.1 General characteristics

Nominal bit rate: 51 840 kbit/s.

Bit rate accuracy: ±20 ppm (±1037 bit/s).

Code: Three line codes may be used:

a) Coded mark inversion (CMI);

b) High density bipolar of order 2 (HDB2) code;

c) High density bipolar of order 3 (HDB3) code.

A description of these codes can be found in Annex A

Overvoltage protection requirements: refer to ITU-T Rec. K.41.

16.2 Specifications at the output ports

The specifications at the output ports are given in Table 13.

Table 13/G.703 – Digital interface at 51 840 kbit/s

Pair(s) in each direction	One coaxial pair
Test load impedance	75 ohms resistive
Maximum peak-to-peak jitter at an output port	1.5 UIpp in the bandwidth from 100 Hz to 400 kHz 0.15 UIpp in the bandwidth from 20 kHz to 400 kHz NOTE 1 – The high-pass measurement filters have a first-order characteristic and a roll-off of –20 dB/decade. The low-pass measurement filters have a maximally flat, Butterworth characteristic and a roll-off of –60 dB/decade. NOTE 2 –The values of jitter for CMI coded STM-0 signals are provisional and should be studied.
If HDB2 or HDB3 codes are used:	
Pulse shape	Nominally rectangular and conforming to the mask (Figure 25) irrespective of the sign. The value V corresponds to the nominal peak value.
Nominal peak voltage of a mark (pulse)	1.0 V
Peak voltage of a space (no pulse)	0 V ± 0.1 V
Nominal pulse width	9.65 ns
Ratio of the amplitudes of positive and negative pulses at the center of a pulse interval	0.95 to 1.05
Ratio of the widths of positive and negative pulses at the nominal half amplitude	0.95 to 1.05
If CMI code is used:	
Pulse shape	Nominally rectangular and conforming to the masks shown in Figures 26 and 27
Peak-to-peak voltage	1 ± 0.1 V
Rise time between 10% and 90% amplitudes of the measured steady state amplitude	≤6 ns
Transition timing tolerance referred to the mean value of the 50% amplitude points of negative transitions	Negative transitions: ±0.3 ns Positive transitions at unit interval boundaries: ±1.5 ns Positive transitions at mid-unit intervals: ±1 ns

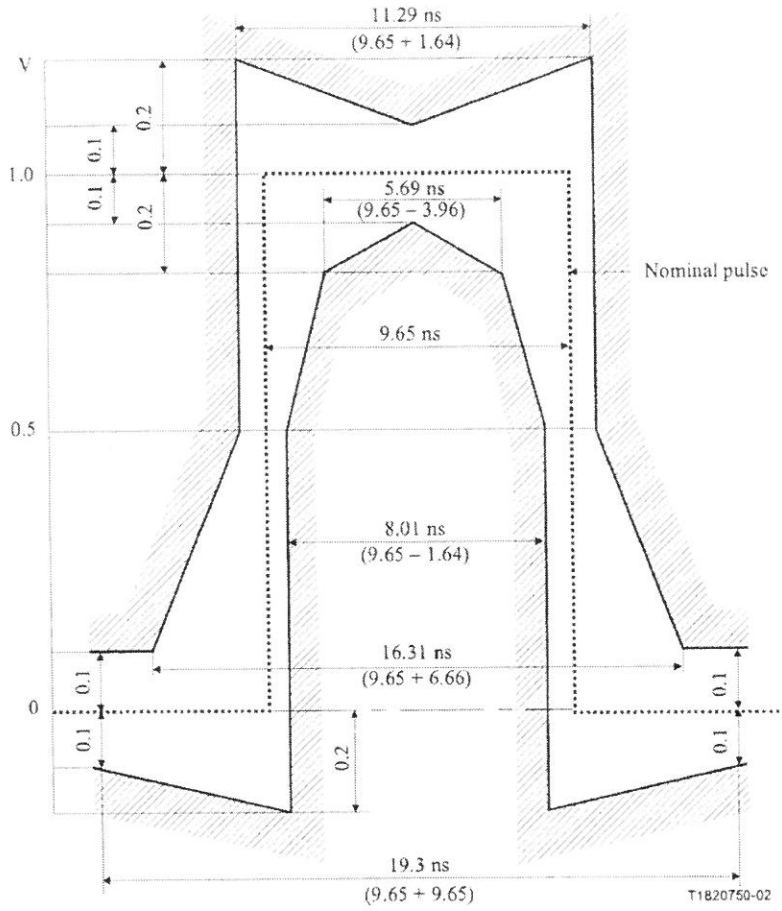
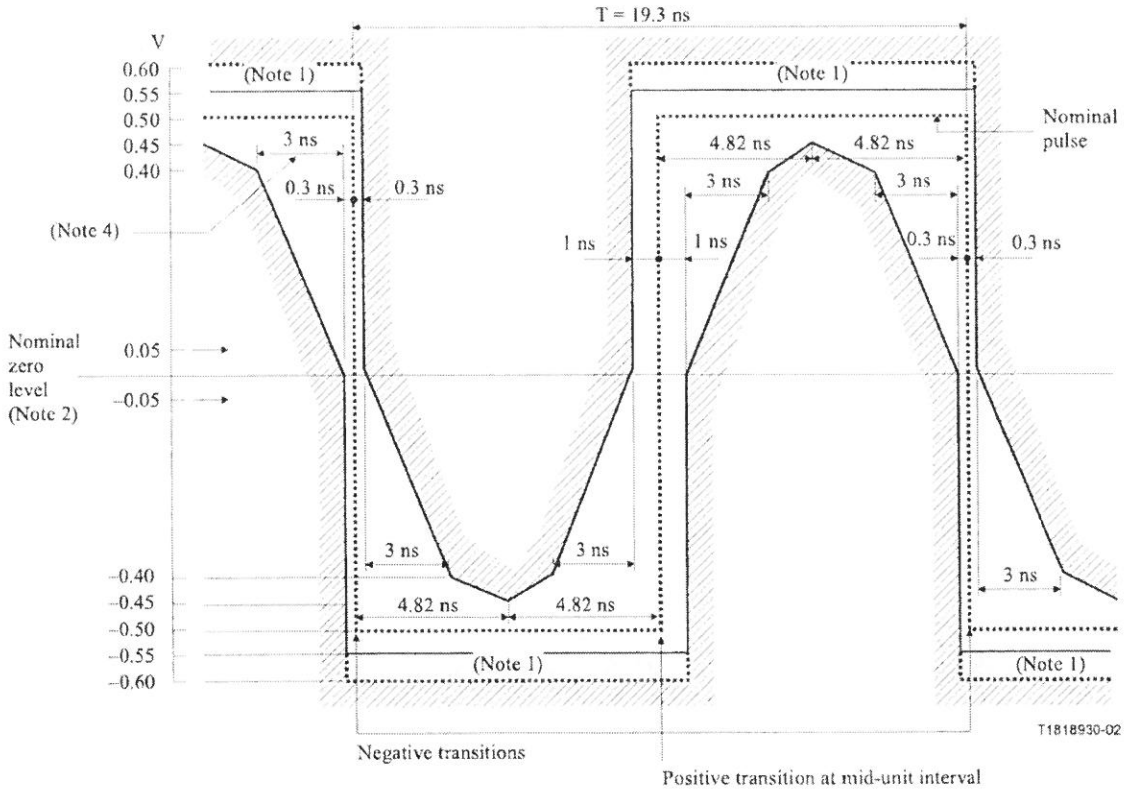


Figure 25/G.703 – Pulse mask at the 51 840 kbit/s interface (if HDB2 or HDB3 codes are used)



NOTE 1 – The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 µF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

NOTE 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident.

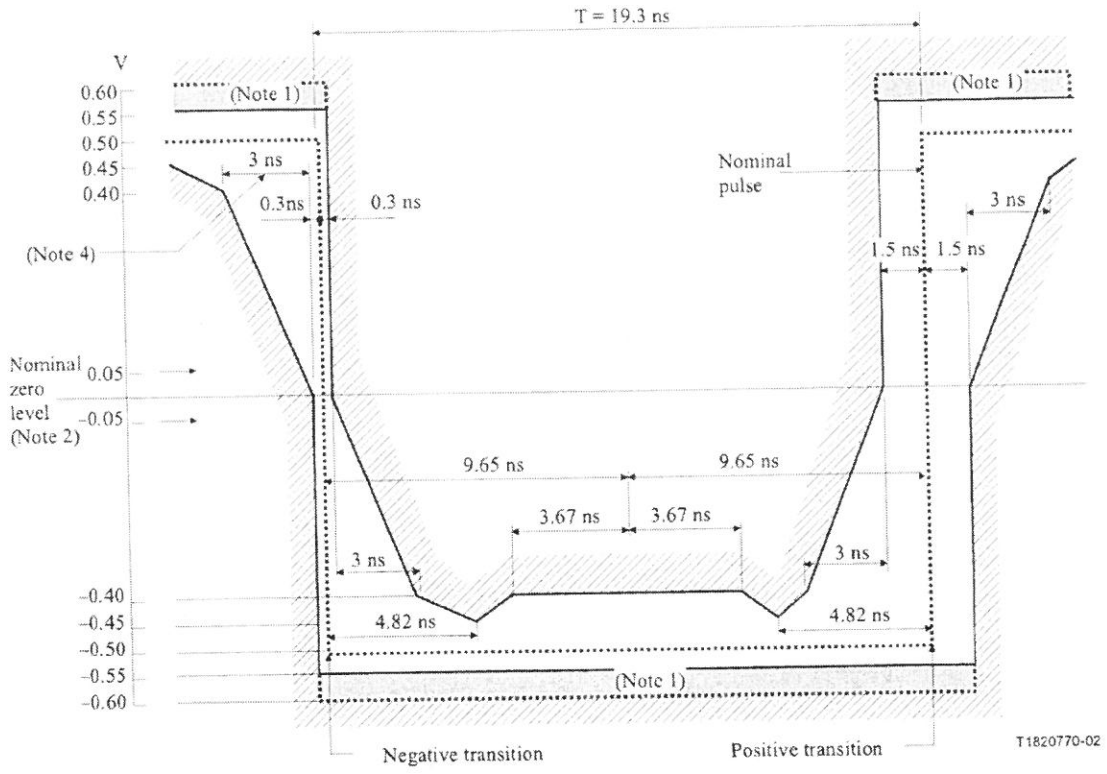
The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.

When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

These techniques require further study.

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between –0.4 V and 0.4 V, and should not exceed 2 ns.

Figure 26/G.703 – Mask of a pulse corresponding to a binary 0 (at the 51 840 kbit/s interface)



NOTE 1 – The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 µF, to the input of the oscilloscope used for measurements.

The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

NOTE 3 – Each pulse in a coded sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident.

The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.

When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of thepulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

These techniques require further study.

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between –0.4 V and 0.4 V, and should not exceed 6 ns.

NOTE 5 – The inverse pulse will have the same characteristics, noting that the timing tolerance at the level of the negative and positive transitions are ±0.3 ns and ±1.5 ns respectively.

Figure 27/G.703 – Mask of a pulse corresponding to a binary 1 (at the 51 840 kbit/s interface)

The return loss at the output port should have the following minimum values:

Frequency range (kHz)	Return loss (dB)
1296 to 2592	6
2592 to 77 760	8

16.3 Specifications at the input ports

The digital signal presented at the input port shall be as defined above but modified by the characteristics of the interconnecting pair. The attenuation of this cable shall be assumed to follow approximately a $\sqrt{f}$ law and the loss at a frequency of 25 920 kHz shall be in the range from 0 to 12 dB.

The return loss at the input port should have the following provisional minimum values:

Frequency range (kHz)	Return loss (dB)
1296 to 2592	12
2592 to 51 840	18
51 840 to 77 760	14

The jitter to be tolerated at the input port expressed in peak-to-peak sinusoidal phase amplitude, shall exceed the values shown in Figure 28:

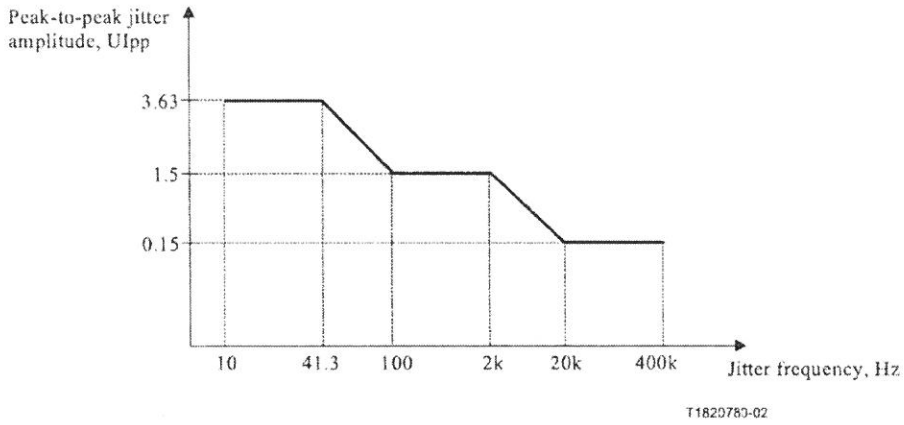


Figure 28/G.703 – 51 840 kbit/s input jitter tolerance limit

NOTE – The values of jitter for CMI coded STM-0 signals are provisional and should be studied.

16.4 Specifications at the cross-connect points

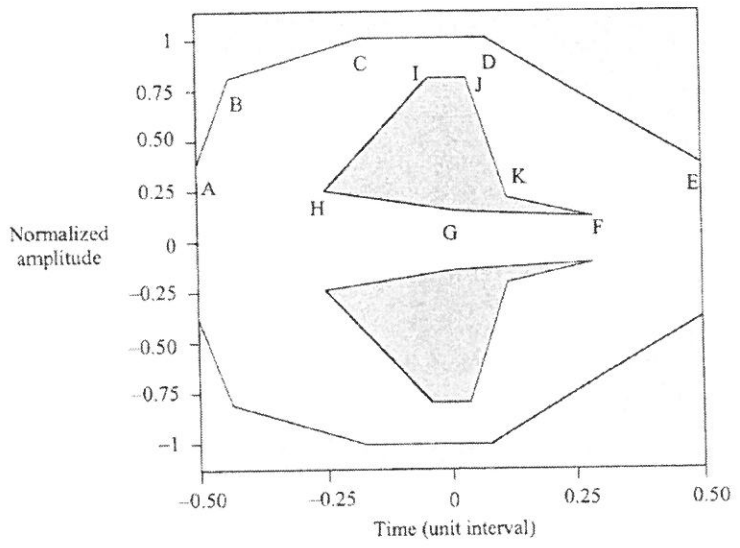
– *Signal power level*

A wideband power measurement using a power level sensor with a working frequency range of at least four times the bit rate frequency shall be between –2.7 and +4.7 dBm, accounting for both transmitter variations and a range of connecting cable lengths between 68.6 m and 137 m. A filter with a characteristic equivalent to a Butterworth low pass filter with a cut-off frequency of 207.360 MHz shall be used.

There shall be no DC power transmitted across the interface.

– *Eye diagram*

An eye diagram mask based on the maximum and minimum power levels and cable lengths given above is shown in Figure 29 where the voltage amplitude has been normalized to one, and the time scale is specified in terms of the unit interval T. Exclusionary regions are shown as shaded areas on the figure. The corner points of these regions are listed below the figure.



Outer region corner points			Inner region corner points		
Point	**Time**	**Amplitude**	**Point**	**Time**	**Amplitude**
A	–0.50	0.37	F	0.28	0.12
B	–0.44	0.80	G	0.00	0.16
C	–0.18	1.00	H	–0.25	0.24
D	0.08	1.00	I	–0.04	0.80
E	0.50	0.37	J	0.04	0.80
			K	0.11	0.22

NOTE – Both inner and outer regions are symmetric about the zero amplitude axis.

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Figure 29/G.703 – STM-0 interface eye diagram

16.5 Grounding of outer conductor

The outer conductor of the coaxial pair shall be connected to the bonding network both at the input port and the output port.

NOTE 1 – The cable routing is important if leaving the system block. Consult ITU-T Rec. K.27 for guidance.

NOTE 2 – The use of isolation to the bonding network is for further study.

Annex A

Definition of codes

This annex defines the modified alternate mark inversion codes (see ITU-T Rec. G.701, item 9005) whose use is specified in this Recommendation.

In these codes, binary 1 bits are generally represented by alternate positive and negative pulses, and binary 0 bits by spaces. Exceptions, as specified for the individual codes, are made when strings of successive 0 bits occur in the binary signal.

In the definitions below, B represents an inserted pulse conforming to the AMI rule (ITU-T Rec. G.701, item 9004), and V represents an AMI violation (ITU-T Rec. G.701, item 9007).

The encoding of binary signals in accordance with the rules given in this annex includes frame alignment bits, etc.

A.1 Definition of B3ZS (also designated HDB2) and HDB3

Each block of 3 (or 4) successive zeros is replaced by 00V (or 000V respectively) or B0V (B00V). The choice of 00V (000V) or B0V (B00V) is made so that the number of B pulses between consecutive V pulses is odd. In other words, successive V pulses are of alternate polarity so that no DC component is introduced.

A.2 Definition of B6ZS and B8ZS

Each block of 6 (or 8) successive zeros is replaced by 0VB0VB (or 000VB0VB respectively).

A.3 Definition of CMI

CMI is a 2-level non-return-to-zero code in which binary 0 is coded so that both amplitude levels, A_1 and A_2, are attained consecutively, each for half a unit time interval (T/2).

Binary 1 is coded by either of the amplitude levels A_1 or A_2, for one full unit time interval (T), in such a way that the level alternates for successive binary 1s.

An example is given in Figure A.1.

NOTE 1 – For binary 0, there is always a positive transition at the midpoint of the binary unit time interval.

NOTE 2 – For binary 1:

a) there is a positive transition at the start of the binary unit time interval if in the preceeding time interval the level was A_1;

b) there is a negative transition at the start of the binary unit time interval if the last binary 1 was encoded by level A_2.

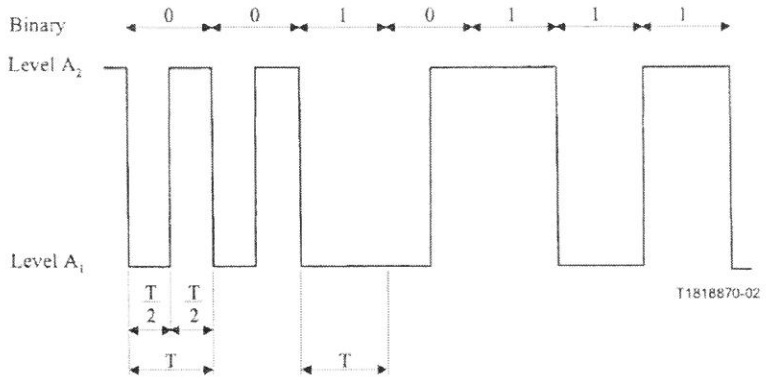


Figure A.1/G.783 – Example of CMI coded binary signal

Appendix I

1544 kbit/s specification in the 1991 version of this Recommendation

I.1 General

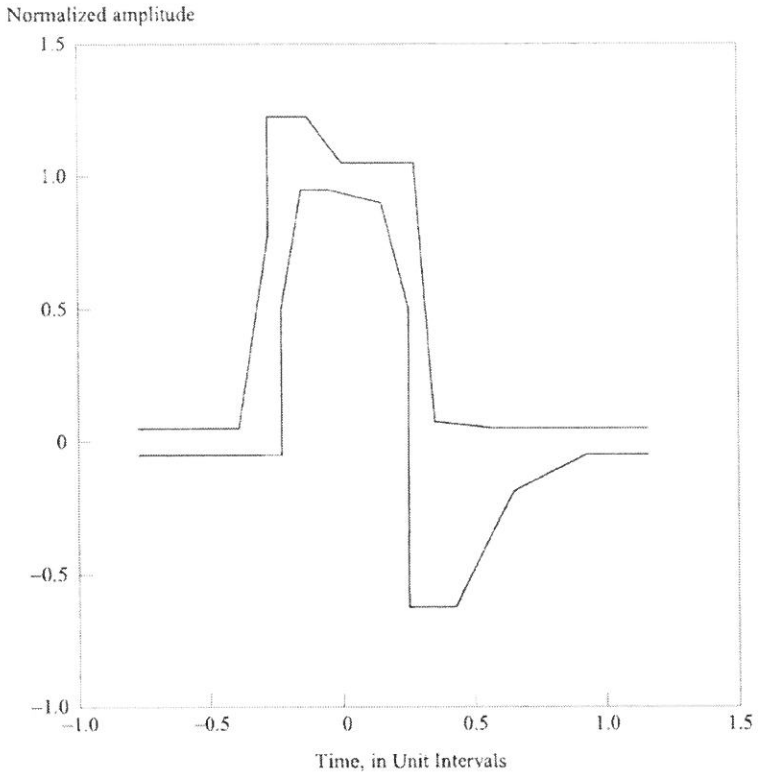
This appendix describes an earlier 1544 kbit/s interface that included a pulse mask with substantially greater allowance for overshoot on the trailing edge of the pulse than the current standard. While the current pulse mask has been socialized in a number of network compatibility publications since the late 1970s, equipment designed to the earlier specification may be widespread in the network. Hence, designers of equipment need to be aware of the nature of signals that may be delivered to that equipment.

I.2 Interface specification

Most of the interface parameters in Table 4, including power levels and pulse amplitudes, apply to the older interface. One major difference is in the line rate tolerance. The older specification calls for a ±130 ppm tolerance, reflecting an earlier, now obsolete, technology for line driver circuitry.

I.3 Pulse mask

Figure I.1 is the 1544 kbit/s pulse mask corresponding to the earlier interface specification. It is based on equipment generating pulses with considerably more overshoot on the trailing edge that is currently allowed in the standard.



Minimum curve		Minimum curve	
Time	Normalized amplitude	Time	Normalized amplitude
– 0.77	– 0.05	– 0.77	0.05
– 0.23	– 0.05	– 0.39	0.05
– 0.23	0.5	– 0.27	0.8
– 0.15	0.95	– 0.27	1.22
– 0.04	0.95	– 0.12	1.22
0.15	0.9	0.0	1.05
0.23	0.5	0.27	1.05
0.23	– 0.62	0.34	0.08
0.42	– 0.62	0.58	0.05
0.66	– 0.2	1.16	0.05
0.93	– 0.05		
1.16	– 0.05		

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Figure I.1/G.703 – Obsolete 1544 kbit/s interface isolated pulse mask and corner points

Appendix II

64 and 6312 kHz synchronization interface specification for use in Japan

II.1 64 kHz synchronization interface

The 64 kHz clock signals from the clock supply equipment have the frequencies of:

a) 64 kHz + 8 kHz or

b) 64 kHz + 8 kHz + 400 Hz.

Those signals consist of AMI code with:

a) an 8 kHz bipolar violation, or

b) an 8 kHz bipolar violation removed at every 400 Hz.

The signal structures of 64 kHz clock signals are illustrated in Figures II.1 and II.2.

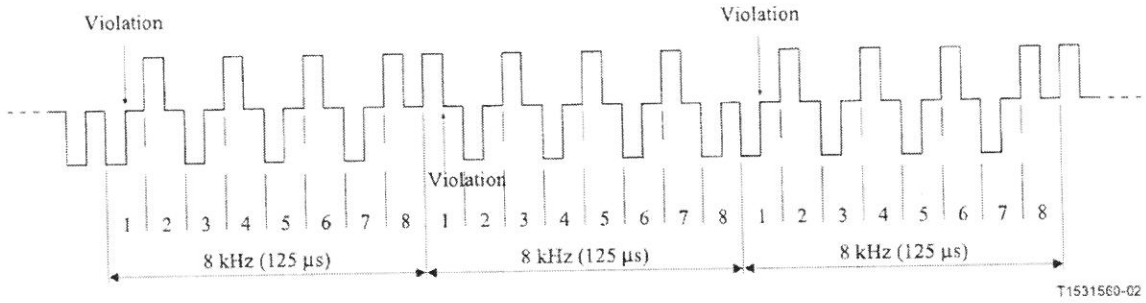

Figure II.1/G.703 – Signal structure of 64 kHz clock interface with a frequency of 64 kHz + 8 kHz

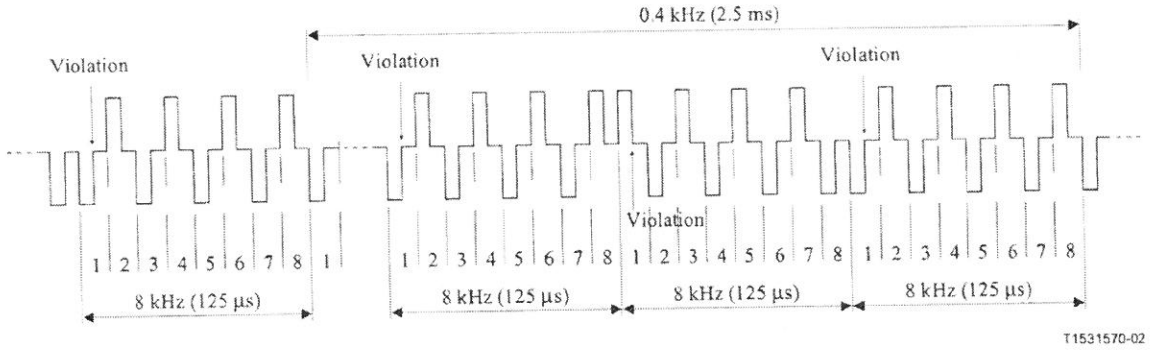

Figure II.2/G.703 – Signal structure of 64 kHz clock interface with a frequency of 64 kHz + 8 kHz + 400 Hz

The specifications of 64 kHz clock signals at input port and output port are shown in Tables II.1 and II.2, respectively.

Table II.1/G.703 – Specification of 64 kHz clock signal at input port

Frequency	a) 64 kHz + 8 kHz or b) 64 kHz + 8 kHz + 400 Hz
	a) AMI with 8 kHz bipolar violation; b) AMI with 8 kHz bipolar violation removed at every 400 Hz
Alarm condition	Alarm should not be occurred against the amplitude ranged 0.63-1.1 $V_{0\text{-}P}$

Table II.2/G.703 – Specification of 64 kHz clock signal at output port

Frequency	a) 64 kHz + 8 kHz or b) 64 kHz + 8 kHz + 400 Hz
Load impedance	110 ohms resistive
Transmission media	Symmetric pair cable
Pulse width (FWHM)	$\leq 7.8 \pm 0.78$ µs
Amplitude	≤ 1 $V_{0\text{-}P} \pm 0.1$ V

II.2 6312 kHz synchronization interface

Figure II.3 shows the waveform of 6312 kHz clock signal. The specifications of 6312 kHz clock signals at input port and output port are shown in Tables II.3 and II.4, respectively.

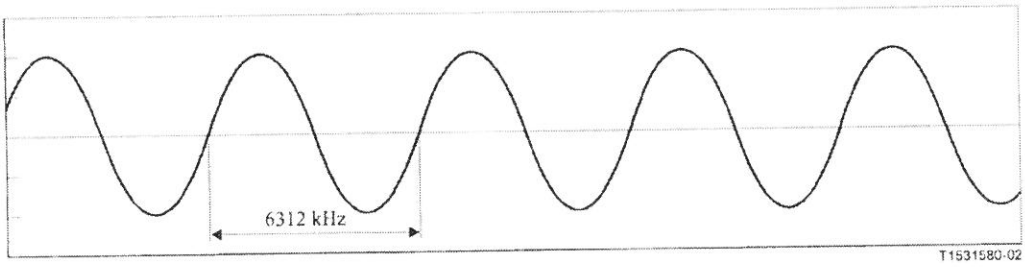

Figure II.3/G.703 – Waveform of 6312 kHz clock signal

Table II.3/G.703 – Specification of 6312 kHz clock signal at input port

Frequency	6312 kHz
Signal format	Sinusoidal wave
Alarm condition	Alarm should not be occurred against the amplitude ranged −16 dBm to +3 dBm

Table II.4/G.703 – Specification of 6312 kHz clock signal at output port

Frequency	6312 kHz
Load impedance	75 ohms resistive
Transmission media	Coaxial pair cable
Amplitude	0 dBm ± 3 dB

Appendix III

3152 kbit/s interface specification for use in North America
(from Annex A/G.931)

Nominal bit rate: 3152 kbit/s.

Bit rate accuracy: ±30 ppm (±95 bit/s).

For specifications at the ports, see Table III.1.

Table III.1/G.703 – Digital interface at 3152 kbit/s

Parameter	Specification
Nominal bit rate	3152 kbit/s
Bit rate accuracy	±30 ppm (±95 bit/s)
Test load impedance	100 ohms ± 5% resistive
Line code	AMI (Notes 1 and 2)
Pulse shape	Nominal rectangular
Pair(s) in each direction of transmission	One balanced twisted pair (Note 3)
Nominal amplitude	3.0 V (Note 4)
Width (at 50% amplitude)	159 ± 30 ns
Rise and fall times (20-80% of amplitude)	≤50 ns (difference between rise and fall times shall be 0 ± 20 ns)
Signal power (all is signal, measured over 10 MHz bandwidth)	16.53 ± 2 dBm [ratio of (power in + pulses) to (power in – pulses) shall be 0 ± 0.5 dB]
NOTE 1 – An AMI code shall be used. For definitions of AMI code; see Annex A/G.703. NOTE 2 – In order to guarantee adequate timing information, the minimum pulse density taken over any 130 consecutive time slots must be 1 in 8. The design intent is that the long-term pulse density be equal to 0.5. In order to provide adequate jitter performance for systems, timing extracting circuits should have a Q of 1200 ± 200 that is representable by a single tuned network. NOTE 3 – One balanced twisted pair shall be used for each direction of transmission. The distribution frame jack connected to a pair bringing signals to the distribution frame is termed the in-jack. The distribution frame jack connected to a pair carrying signals away from the distribution frame is termed the out-jack. NOTE 4 – The peak-to-peak voltage within a time slot containing a zero (space) produced by other pulses meeting the specifications of Table III.1 should not exceed 0.1 of the peak pulse amplitude.	

Requirements for the maximum peak-to-peak jitter at the output port and the jitter to be tolerated at the input port are for further study.

Overvoltage protection requirements: refer to ITU-T Rec. K.41.

SERIES OF ITU-T RECOMMENDATIONS

Series A	Organization of the work of ITU-T
Series B	Means of expression: definitions, symbols, classification
Series C	General telecommunication statistics
Series D	General tariff principles
Series E	Overall network operation, telephone service, service operation and human factors
Series F	Non-telephone telecommunication services
Series G	**Transmission systems and media, digital systems and networks**
Series H	Audiovisual and multimedia systems
Series I	Integrated services digital network
Series J	Cable networks and transmission of television, sound programme and other multimedia signals
Series K	Protection against interference
Series L	Construction, installation and protection of cables and other elements of outside plant
Series M	TMN and network maintenance: international transmission systems, telephone circuits, telegraphy, facsimile and leased circuits
Series N	Maintenance: international sound programme and television transmission circuits
Series O	Specifications of measuring equipment
Series P	Telephone transmission quality, telephone installations, local line networks
Series Q	Switching and signalling
Series R	Telegraph transmission
Series S	Telegraph services terminal equipment
Series T	Terminals for telematic services
Series U	Telegraph switching
Series V	Data communication over the telephone network
Series X	Data networks and open system communications
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Series Z	Languages and general software aspects for telecommunication systems

Geneva, 2002

Exhibit E

COVERING NOTE

GENERAL SECRETARIAT OF THE INTERNATIONAL TELECOMMUNICATION UNION

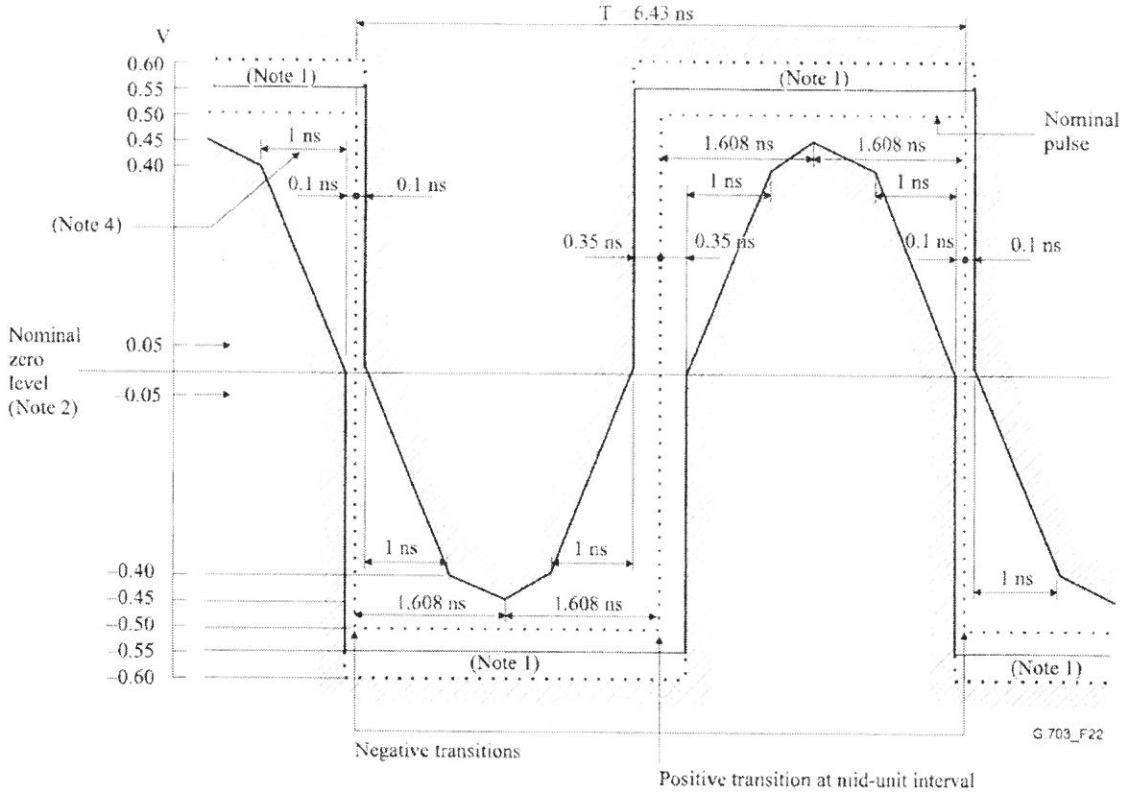
Geneva, 20 July 2005

ITU – TELECOMMUNICATION
STANDARDIZATION SECTOR

Subject: Erratum 1 (07/2005) to

ITU-T Recommendation G.703 (11/2001), *Physical/electrical characteristics of hierarchical digital interfaces*

1) In Figure 22/G.703 "Mask of a pulse corresponding to a binary 0 (at the 155 520 kbit/s interface)", mask values were incorrect (pulse period of 19.3 ns instead of 6.43 ns). Replace the whole figure by the following:



NOTE 1 – The maximum "steady state" amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.

NOTE 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 μF, to the input of the oscilloscope used for measurements.
The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed ±0.05 V. This may be checked by removing the input signal again and verifying that the trace lies within ±0.05 V of the nominal zero level of the masks.

NOTE 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident.
The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal.
When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal]. These techniques require further study.

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between –0.4 V and 0.4 V, and should not exceed 2 ns.

2) In Figure 26/G.703 "Mask of a pulse corresponding to a binary 0 (at the 51 840 kbit/s interface)", correct Note 4 as follows:

NOTE 4 – For the purpose of these masks, the rise time and decay time should be measured between –0.4 V and 0.4 V, and should not exceed ~~2~~ 26 ns.

EXHIBIT F

International Telecommunication Union

ITU-T

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

G.703

Corrigendum 1

(03/2008)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital terminal equipments – General

Physical/electrical characteristics of hierarchical digital interfaces

Corrigendum 1

ITU-T Recommendation G.703 (2001) – Corrigendum 1

ITU-T

ITU-T G-SERIES RECOMMENDATIONS

TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

INTERNATIONAL TELEPHONE CONNECTIONS AND CIRCUITS	G.100–G.199
GENERAL CHARACTERISTICS COMMON TO ALL ANALOGUE CARRIER-TRANSMISSION SYSTEMS	G.200–G.299
INDIVIDUAL CHARACTERISTICS OF INTERNATIONAL CARRIER TELEPHONE SYSTEMS ON METALLIC LINES	G.300–G.399
GENERAL CHARACTERISTICS OF INTERNATIONAL CARRIER TELEPHONE SYSTEMS ON RADIO-RELAY OR SATELLITE LINKS AND INTERCONNECTION WITH METALLIC LINES	G.400–G.449
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Coding of analogue signals by methods other than PCM	G.720–G.729
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Principal characteristics of second order multiplex equipment	G.740–G.749
Principal characteristics of higher order multiplex equipment	G.750–G.759
Principal characteristics of transcoder and digital multiplication equipment	G.760–G.769
Operations, administration and maintenance features of transmission equipment	G.770–G.779
Principal characteristics of multiplexing equipment for the synchronous digital hierarchy	G.780–G.789
Other terminal equipment	G.790–G.799
DIGITAL NETWORKS	G.800–G.899
DIGITAL SECTIONS AND DIGITAL LINE SYSTEM	G.900–G.999
QUALITY OF SERVICE AND PERFORMANCE – GENERIC AND USER-RELATED ASPECTS	G.1000–G.1999
TRANSMISSION MEDIA CHARACTERISTICS	G.6000–G.6999
DATA OVER TRANSPORT – GENERIC ASPECTS	G.7000–G.7999
PACKET OVER TRANSPORT ASPECTS	G.8000–G.8999
ACCESS NETWORKS	G.9000–G.9999

For further details, please refer to the list of ITU-T Recommendations.

ITU-T Recommendation G.703

Physical/electrical characteristics of hierarchical digital interfaces

Corrigendum 1

Summary

This corrigendum contains material to correct ITU-T Recommendation G.703 (2001), *Physical/electrical characteristics of hierarchical digital interfaces*.

Source

Corrigendum 1 to ITU-T Recommendation G.703 (2001) was approved on 29 March 2008 by ITU-T Study Group 15 (2005-2008) under the ITU-T Recommendation A.8 procedure.

FOREWORD

The International Telecommunication Union (ITU) is the United Nations specialized agency in the field of telecommunications, information and communication technologies (ICTs). The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of ITU. ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

The approval of ITU-T Recommendations is covered by the procedure laid down in WTSA Resolution 1.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Compliance with this Recommendation is voluntary. However, the Recommendation may contain certain mandatory provisions (to ensure e.g. interoperability or applicability) and compliance with the Recommendation is achieved when all of these mandatory provisions are met. The words "shall" or some other obligatory language such as "must" and the negative equivalents are used to express requirements. The use of such words does not suggest that compliance with the Recommendation is required of any party.

INTELLECTUAL PROPERTY RIGHTS

ITU draws attention to the possibility that the practice or implementation of this Recommendation may involve the use of a claimed Intellectual Property Right. ITU takes no position concerning the evidence, validity or applicability of claimed Intellectual Property Rights, whether asserted by ITU members or others outside of the Recommendation development process.

As of the date of approval of this Recommendation, ITU had not received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementers are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database at http://www.itu.int/ITU-T/ipr/.

ITU-T Recommendation G.703

Physical/electrical characteristics of hierarchical digital interfaces

Corrigendum 1

Modify Table 11 as shown:

Table 11/G.703 – Digital 2048 kHz clock interface

Pulse shape	The signal must conform with the mask (Figure 20). The value V corresponds to the maximum peak value. The value V_1 corresponds to the minimum peak value.	
Type of pair	Coaxial pair (see Note in 13.4)	Symmetrical pair (see Note in 13.4)
Test load impedance	75 ohms resistive	120 ohms resistive
Maximum peak voltage (V_{ep})	1.5	1.9
Minimum peak voltage ~~(V_{op})~~ (V_1)	0.75	1.0
Maximum jitter at an output port	Refer to Table 5/G.823 (Note)	
NOTE – This value is valid for network timing synchronization equipments. Other values may be specified for timing output ports of digital links carrying the network timing.		

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Printed in Switzerland
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EXHIBIT G

International Telecommunication Union

ITU-T

TELECOMMUNICATION
STANDARDIZATION SECTOR
OF ITU

G.703

Amendment 1
(08/2013)

SERIES G: TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

Digital terminal equipments – General

Physical/electrical characteristics of hierarchical digital interfaces

Amendment 1 – Specifications for the physical layer of the new ITU-T G.8271/Y.1366 time synchronization interfaces

Recommendation ITU-T G.703 (2001) – Amendment 1

ITU-T

International Telecommunication Union

ITU-T G-SERIES RECOMMENDATIONS

TRANSMISSION SYSTEMS AND MEDIA, DIGITAL SYSTEMS AND NETWORKS

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GENERAL CHARACTERISTICS COMMON TO ALL ANALOGUE CARRIER-TRANSMISSION SYSTEMS	G.200–G.299
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Principal characteristics of multiplexing equipment for the synchronous digital hierarchy	G.780–G.789
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PACKET OVER TRANSPORT ASPECTS	G.8000–G.8999
ACCESS NETWORKS	G.9000–G.9999

For further details, please refer to the list of ITU-T Recommendations.

Recommendation ITU-T G.703

Physical/electrical characteristics of hierarchical digital interfaces

Amendment 1

Specifications for the physical layer of the new ITU-T G.8271/Y.1366 time synchronization interfaces

Summary

Amendment 1 to Recommendation ITU-T G.703 (2001) adds specifications for the physical layer of the new time synchronization interfaces defined in Recommendation ITU-T G.8271/Y.1366.

History

Edition	Recommendation	Approval	Study Group
1.0	ITU-T G.703	1972-12-15	
2.0	ITU-T G.703	1976-10-08	
3.0	ITU-T G.703	1980-11-21	
4.0	ITU-T G.703	1984-10-19	
5.0	ITU-T G.703	1988-11-25	
6.0	ITU-T G.703	1991-04-05	XVIII
7.0	ITU-T G.703	1998-10-13	15
8.0	ITU-T G.703	2001-11-29	15
8.1	ITU-T G.703 (2001) Cor. 1	2008-03-29	15
8.2	ITU-T G.703 (2001) Amd. 1	2013-08-29	15

FOREWORD

The International Telecommunication Union (ITU) is the United Nations specialized agency in the field of telecommunications, information and communication technologies (ICTs). The ITU Telecommunication Standardization Sector (ITU-T) is a permanent organ of ITU. ITU-T is responsible for studying technical, operating and tariff questions and issuing Recommendations on them with a view to standardizing telecommunications on a worldwide basis.

The World Telecommunication Standardization Assembly (WTSA), which meets every four years, establishes the topics for study by the ITU-T study groups which, in turn, produce Recommendations on these topics.

The approval of ITU-T Recommendations is covered by the procedure laid down in WTSA Resolution 1.

In some areas of information technology which fall within ITU-T's purview, the necessary standards are prepared on a collaborative basis with ISO and IEC.

NOTE

In this Recommendation, the expression "Administration" is used for conciseness to indicate both a telecommunication administration and a recognized operating agency.

Compliance with this Recommendation is voluntary. However, the Recommendation may contain certain mandatory provisions (to ensure, e.g., interoperability or applicability) and compliance with the Recommendation is achieved when all of these mandatory provisions are met. The words "shall" or some other obligatory language such as "must" and the negative equivalents are used to express requirements. The use of such words does not suggest that compliance with the Recommendation is required of any party.

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As of the date of approval of this Recommendation, ITU had not received notice of intellectual property, protected by patents, which may be required to implement this Recommendation. However, implementers are cautioned that this may not represent the latest information and are therefore strongly urged to consult the TSB patent database at http://www.itu.int/ITU-T/ipr/.

Recommendation ITU-T G.703

Physical/electrical characteristics of hierarchical digital interfaces

Amendment 1

Specifications for the physical layer of the new ITU-T G.8271/Y.1366 time synchronization interfaces

1) Introduction

This amendment adds specifications for the physical layer of the new time synchronization interfaces defined in ITU-T G.8271/Y.1366.

2) Additions

2.1) References

Add the following reference to clause 2:

[ITU-T G.8271] Recommendation ITU-T G.8271/Y.1366 (2012), *Time and phase synchronization aspects of packet networks.*

[ITU-T V.11] Recommendation ITU-T V.11 (1996), *Electrical characteristics for balanced double-current interchange circuits operating at data signalling rates up to 10 Mbit/s.*

[IEC 60603-7] IEC 60603-7 ed3.1 Consol. with am1 (2011-12), *Connectors for electronic equipment - Part 7: Detail specification for 8-way, unshielded, free and fixed connectors.*

2.2) Abbreviations

Add the following abbreviations to clause 3:

GND Ground

GNSS Global Navigation Satellite System

1PPS One Pulse Per Second

2.3) New clause 17

Add the following new clause 17:

17 Time synchronization interfaces defined in ITU-T G.8271/Y.1366

17.1 ITU-T V.11-based time/phase distribution interface

The ITU-T V.11-based time/phase distribution interface provides an indication of the time of day and the one pulse per second (1PPS) signal as a phase indication. The expected physical connector is commonly referred to as the RJ-45 connector [IEC 60603-7].

The 1PPS time/phase interface uses a point-to-point ITU-T V.11 interface as specified in [ITU-T V.11] with an additional requirement on the rise and fall times of the 1PPS signal. This is needed to provide the accuracy required for the 1PPS signal.

This interface can be used for time synchronization distribution as well as for time measurement.

The interface is a balanced interface that can tolerate significant common mode noise.

The 1PPS interface consists of a balanced 100 ohm 1PPS differential signal that can be used to connect to another timing device or to measurement equipment.

The following mapping of signals is defined for use with the RJ-45 connector:

Two modes are supported:

1) Time input mode (the unit receives a time synchronization signal from an external time sync master).

2) Time output mode (the unit outputs a time synchronization signal towards an interface). The receiver of this time sync signal would be a unit operating in time input mode. This could be either test equipment or a time slave clock.

In the event that both time input and time output modes are required at the same time, two RJ-45 connectors are required.

Table 17-1 – RJ-45 connector operating in time input mode

PIN	Signal name	Signal definition
1	Reserved	For further study
2	Reserved	For further study
3	1PPS_IN–	Rx 1PPS negative voltage
4	GND	ITU-T V.11 signal ground
5	User defined	Note
6	1PPS_IN+	Rx 1PPS positive voltage
7	RX–	Rx TOD time message negative voltage
8	RX+	Rx TOD time message positive voltage
NOTE – One possible use of Pin 5 may be ground (GND). An alternative use for this pin could be considered when connected to GNSS receivers. This is out of the scope of this Recommendation. If the signal is not used, it is recommended to pull it down with a resistor of 10 kΩ.		

Table 17-2 – RJ-45 connector operating in time output mode

PIN	Signal name	Signal definition
1	Reserved	For further study
2	Reserved	For further study
3	1PPS_OUT–	Tx 1PPS negative voltage
4	GND	ITU-T V.11 signal ground
5	GND (Note)	ITU-T V.11 signal ground
6	1PPS_OUT+	Tx 1PPS positive voltage
7	TX–	Tx TOD time message negative voltage
8	TX+	Tx TOD time message positive voltage
NOTE – The time interface discussed in this Recommendation generally concerns transport equipment. For the time output mode interface of a GNSS receiver, similar considerations concerning Pin 5 to those made in the Note to Table 17-1 would be required.		

If only one mode is required, a single RJ-45 can be used and configured as time input or time output mode:

Table 17-3 – RJ-45 connector when only one mode is used

PIN	Signal name – Time input configuration	Signal name – Time output configuration	Signal definition
1	Reserved (Note 1)	Reserved	For further study
2	Reserved (Note 1)	Reserved	For further study
3	1PPS_IN–	1PPS_OUT–	Rx or Tx 1PPS negative voltage
4	GND	GND	ITU-T V.11 signal ground
5	User defined (Note 2)	GND	Note 2
6	1PPS_IN+	1PPS_OUT+	Rx or Tx 1PPS positive voltage
7	RX–	TX–	Rx or Tx TOD time message negative voltage
8	RX+	TX+	Rx or Tx TOD time message positive voltage

NOTE 1 – The use of Pin 1 and Pin 2 is not yet defined. They may be used for the measurement of 1PPS signal delay or may be used for configuring a GNSS receiver unit. Pin 1 and Pin 2 may be differential signals.

NOTE 2 – One possible use of Pin 5 in the input configuration may be GND. Alternative usage could be considered when connected to GPS receivers. This is out of the scope of this Recommendation. If the signal is not used, it is recommended to pull it down with a resistor of 10 kΩ.

17.1.1 1PPS rise and fall time specification

The maximum rise and fall times of the 1PPS_OUT signal pair at the output port are more stringent than those specified in clause 5.3 of [ITU-T V.11]. Values are for further study. The positive pulse width must be between 100 ns and 500 ms.

17.1.2 Signal timing

The time master must generate a positive pulse on the 1PPS signal such that the midpoint of the leading edge of the differential ITU-T V.11 signal at the edge of the chassis occurs at the change of the one-second time of the system.

The cable delays of the 1PPS signal must be controlled and compensated if needed in the receiving side so as to meet the requirements stated in Table 17-4. This may be done either manually by the network operator or automatically by the equipment.

Table 17-4 – Timing budget for time distribution of the 1PPS interface

Parameter	Tolerance	Reference point
1PPS signal generation accuracy of the timing master	±10 ns	
Cable delay compensation accuracy (Note 1)	±10 ns	From connector to connector with an ITU-T V.11 pulse
1PPS signal detection accuracy at the slave	Note 2	

NOTE 1 – The applicable cable length is for further study (values between 3 m and 1000 m have been proposed; contributions are invited).

NOTE 2 – A range between 10 and 30 ns has been mentioned, and 30 ns are agreed as worst case.

NOTE 3 – The specification of the rise and fall time is for further study.

17.2 1PPS 50 Ω phase-synchronization measurement interface

The 1PPS interface consists of an unbalanced 50 ohm 1PPS signal that can be used to connect to measurement equipment.

NOTE – The unbalanced 50 ohm 1PPS measurement output may be used for phase distribution assuming that the distribution interface complies with the limits set in Table 17-4. If time distribution is required, an additional interface is required in order to transfer the corresponding time synchronization information. This additional interface is out of the scope of this Recommendation.

As an example, a 1PPS interface consisting of an unbalanced 50 ohm signal has been used as the distribution interface in some legacy equipment that only required phase/frequency synchronization.

17.2.1 Performance specification

This signal indicates the significant event occurring on the midpoint of the leading edge of the signal.

The system must generate a positive pulse on the 1PPS signal such that the midpoint of the leading edge of the signal at the edge of the chassis occurs at the one second roll-over of the system.

The pulse width must be between 100 ns and 500 ms.

The 10-90% rise times of the 1PPS pulse should be < 5 ns.

This interface is intended to be used with an impedance controlled 50 ohm cable with a maximum length of three metres to keep the influence of delay and rise time low.

Table 17-5 – Timing specification for the 1PPS measurement interface

Parameter	Tolerance	Comment
1PPS signal generation accuracy of the timing master	±5 ns	Measured at the 50% amplitude level
Maximum cable length	3 m	Due to delay and rise time performance

17.2.2 Voltage levels

Table 17-6 gives voltage levels for the interface for information.

Table 17-6 – Output voltage levels

Interface	VOH (max)	VOH (min)	VOL (max)	VOL (min)
1PPS (50 ohm single-ended)	5.5 V	1.2 V	0.3 V	–0.3 V
NOTE – Measured with a 50 ohm load to ground.				

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EXHIBIT H

The Fundamentals of DS3

Overview

To meet the growing demands of voice and data communications, America's largest corporations are exploring the high-speed worlds of optical fiber and DS3 circuits. As end-users continue to demand more throughput, the move to DS3 circuits is often the best solution for DS1-based private networks. Today's DS3 tariff rates are designed to attract customers, even if these customers can't immediately take advantage of the extra bandwidth. And, depending on location and distance, a DS3 circuit will cost about the same amount as four to 10 DS1 circuits. Once the jump to DS3 bandwidth is made, users have a cost-effective means to implement a host of new communication technologies including video conferencing, workstation-based graphics, distributed data processing, and more advanced facsimile transmission.

Because of the increasing presence of DS3 circuits, understanding the DS3 channel is imperative. This ***Technical Note*** provides a detailed description of how the DS3 channel is formed or multiplexed from 28 separate DS1 channels. It is assumed that the reader has a basic understanding of the DS1 framing format.

The multiplexing involved in forming a DS3 signal is a two-step process. First, the 28 DS1 signals are multiplexed into seven separate DS2 signals, where each DS2 signal contains four DS1 signals. Second, the seven DS2 signals are combined to form the DS3 signal.

DS1 Framing Format Review

To review very briefly, the DS1 frame contains 24 8-bit DS0 channels and a framing bit for a total of 193 bits in the frame. Each 8-bit DS0 channel operates at a sampling rate of 8 kHz, which is also the DS1 frame rate. Therefore, the total aggregate bit rate for DS1 is:

193 bits/frame x 8,000 frame/sec = 1.544 Mbps

which is the nominal bit rate for DS1.

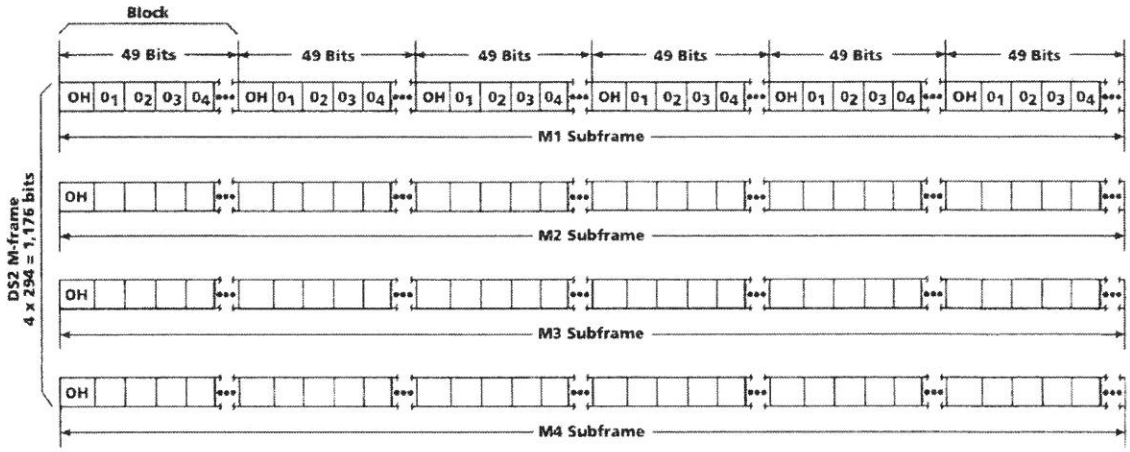
DS2 Framing Format

The first step in the two-step DS1-to-DS3 multiplexing process is to form a DS2 signal by combining four DS1 signals. ***Figure 1*** on the next page shows the DS2 framing format. The DS2 frame (sometimes called a DS2 M-frame) is composed of four subframes, designated M1 thru M4. Each subframe consists of six blocks and each block contains 49 bits. The first bit in each block is a DS2 overhead (OH) bit. Each DS2 frame contains 24 of these OH bits (1 OH bit/block x 6 blocks/subframe x 4 subframes/DS2 frame). The remaining 48 bits in a block are DS1 information bits. The total number of DS1 information bits in a DS2 frame is:

48 DS1 bits/block x 6 blocks/subframe x
4 subframes/DS2 frame = 1,152 DS1 information bits

The four subframes do *not* represent each of the separate DS1 signals. Rather, the DS2 frame is formed by bit-by-bit interleaving the four DS1 signals, as demonstrated in ***Figure 1***.

The OH bit leads off every block and is followed by the interleaved DS1 data bits where 0_i designates the time slot devoted to DS1 input i. After every 48 DS1



NOTES:
1. 0_i designates a time slot devoted to DS1 input i as part of the bit-by-bit interleaving process.
2. 6 blocks/M-subframe x 49 bits/block = 294 bits/M-subframe.

Figure 1
DS2 framing format.

information bits, 12 from each DS1 signal, a DS2 OH bit is inserted. The total number of DS1 information bits transmitted in one second in a DS2 frame is:

DS1 rate x 4 DS1 signals per DS2 which is
1.544 Mbps x 4 DS1 signals/DS2 = 6.176 Mbps

The overall rate chosen for DS2 is 6.312 Mbps. The reason this rate is chosen is to provide extra bandwidth for DS2 bit stuffing and DS2 OH bits as explained below.

DS2 Bit Stuffing

The four DS1 signals are asynchronous relative to each other, and therefore may be operating at different rates. A synchronization method used by multiplexers, called bit stuffing (or pulse stuffing[1]), is used to adjust the different incoming rates. Bit stuffing is explained in greater detail in the Bit Stuffing sidebar on page 4.

DS2 OH Bits

The DS2 OH bits provide alignment and bit stuffing control. The OH bits are located in the first bit position of every block. ***Figure 2*** shows the location of the various DS2 overhead bits designated F, M, and C.

F-bits

The F-bits (framing bits) form the frame alignment signal. There are eight F-bits per DS2 frame (two

[1]Bell Laboratories. *Transmission Systems for Communications*. (Holmdel, N.J.: Bell Telephone Laboratories, Inc., 1982), pp. 675-680.

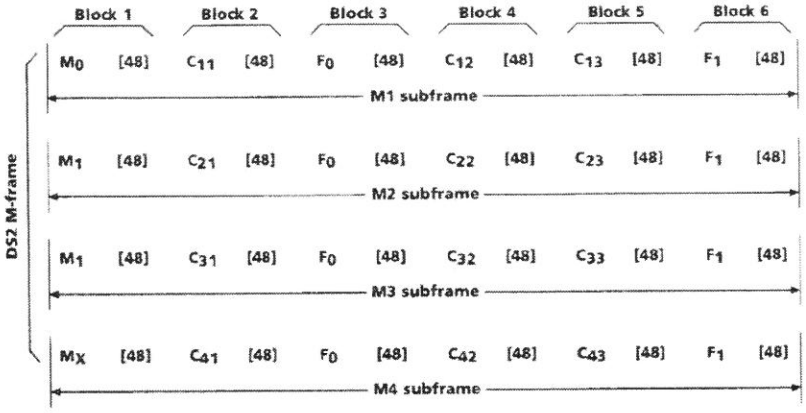


Figure 2
DS2 overhead bits.

Notes:

1. F_0F_1 is the frame alignment signal. $F_0 = 0$ and $F_1 = 1$.
2. $M_0M_1M_1M_X$ is the multiframe alignment signal. $M_0 = 0$, $M_1 = 1$, and M_X may be a 0 or a 1.
3. $C_{11}C_{12}C_{13}$ = stuffing indicators for DS1 input 1.
   $C_{21}C_{22}C_{23}$ = stuffing indicators for DS1 input 2.
   $C_{31}C_{32}C_{33}$ = stuffing indicators for DS1 input 3.
   $C_{41}C_{42}C_{43}$ = stuffing indicators for DS1 input 4.
   If the three C-bits in subframe i are all zeros, no stuffing was done for DS1 input i. If the three C-bits are all ones, stuffing was done.
4. [48] represents 48 DS1 information bits between every DS2 OH bit.

per subframe). The F-bits are located in the first bit position in blocks 3 and 6 of each subframe. The frame alignment pattern, which is repeated every subframe, is "01".

The rate of framing bit errors is a good in-service approximation of the logic bit error rate because of the number and location of framing bits.

M-bits

The M-bits (multiframing bits) form the multiframe alignment signal. There are four M-bits per DS2 frame (one per subframe). The M-bits are located in the first bit position in each subframe. Transmission equipment uses the M-bit pattern, "011X", (where X can be a "0" or a "1") to locate the four subframes.

C-bits

The C-bits are used to control bit stuffing. There are three C-bits per subframe, designated C_{ij} (see ***Figure 2***), where i corresponds to the subframe number and j refers to the position number of the C-bit in a particular subframe. Refer to Appendix A on page 10 for details on how the C-bits are used to control bit stuffing within the DS2 frame.

Bit Stuffing Basics

Bit stuffing is a synchronization method used by multiplexers to adjust for different incoming rates. Bit stuffing works by making the overall output rate high enough to handle a range of input rates. For example, four DS1 signals multiplexed into a DS2 signal require the following minimum bandwidth:

4 x 1.544 Mbps (nominal DS1)	6,176,000 bps
DS2 OH bits	+128,816 bps
Total minimum DS2 bandwidth	6,304,816 bps

The output rate normally chosen for DS2 is 6.312 Mbps which is an even multiple of the 8 kHz sampling rate and provides extra bandwidth beyond the minimum requirement of 6,304,816 bps. The extra bandwidth is used to accommodate bit stuffing for each incoming DS1 signal until each rate is increased to an "intermediate" rate of 1,545,796 bps. Taking the sum of the four "intermediate" DS1 rates along with the DS2 OH bits gives the DS2 aggregate output rate of 6.312 Mbps. During the multiplexing process the stuffed bits are inserted at fixed locations in the framing format, and are identified and removed during demultiplexing.

The output rate chosen for DS3 is 44.736 Mbps which is also an even multiple of the 8 kHz sampling rate and provides the extra bandwidth necessary for bit stuffing at the DS3 level. Complete details on the mechanics of bit stuffing, for the standard M13 asynchronous format, at the DS2 and DS3 levels are provided in Appendices A and B, on pages 10 and 13, respectively. Appendix C on page 16 covers bit stuffing for the C-bit parity format.

DS3 Framing Format

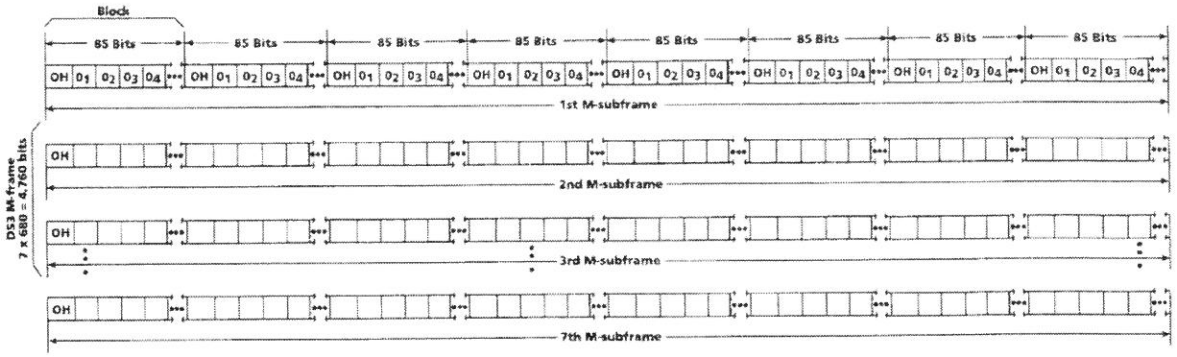
The second step in forming a DS3 signal is to multiplex seven DS2 signals (each containing four DS1 signals) into a DS3 signal. The same method that is used to multiplex the four DS1 signals into a DS2 signal applies. ***Figure 3*** shows the DS3 framing format, known as the standard M13 asynchronous format. M13 is the multiplex designation for multiplexing 28 DS1 signals into one DS3 signal. The DS3 frame (sometimes called a DS3 M-frame) is composed of seven subframes, designated 1st thru 7th. Each subframe consists of eight blocks and each block contains 85 bits. The first bit in each block is a DS3 OH bit. Each DS3 frame contains 56 of these OH bits (1 OH bit/block x 8 blocks/subframe x 7 subframes/DS3 frame). The remaining 84 bits in a block are DS2 information bits. The total number of DS2 information bits in a DS3 frame is:

84 DS2 bits/block x 8 blocks/subframe x
7 subframes/DS3 frame = 4,704 DS2 information bits

The seven subframes do *not* represent each of the separate DS2 signals. Instead, the DS3 frame is formed by bit-by-bit interleaving the seven DS2 signals, as demonstrated in ***Figure 3***. This interleaving process is the same as that used when the four DS1 signals are multiplexed together to form a DS2 signal. After every 84 DS2 information bits, 12 from each DS2 signal, a DS3 OH bit is inserted. The total number of DS2 information bits transmitted in one second is:

DS2 rate x 7 DS2 signals per DS3 which is
6.312 Mbps x 7 DS2 signals = 44.184 Mbps

The overall rate chosen for DS3 is 44.736 Mbps. The reason this rate is chosen is to provide extra bandwidth for DS3 bit stuffing and DS3 OH bits as explained on the next page.



NOTES:
1. 0_i designates a time slot devoted to DS2 input i.
2. 8 blocks/M-subframe x 85 bits/block = 680 bits/M-subframe.

Figure 3
DS3 framing format.

DS3 Bit Stuffing

The seven DS2 signals may be asynchronous relative to each other (because they may not have been formed within a common multiplexer) and therefore may be operating at different rates. Bit stuffing, again, is used to adjust the different incoming rates. Bit stuffing is explained in greater detail in the Bit Stuffing sidebar.

DS3 OH Bits

The DS3 OH bits provide alignment, error checking, in-band communications, and bit stuffing control information. The OH bits are located in the first bit position of every block. ***Figure 4*** on the next page shows the location of the various DS3 OH bits.

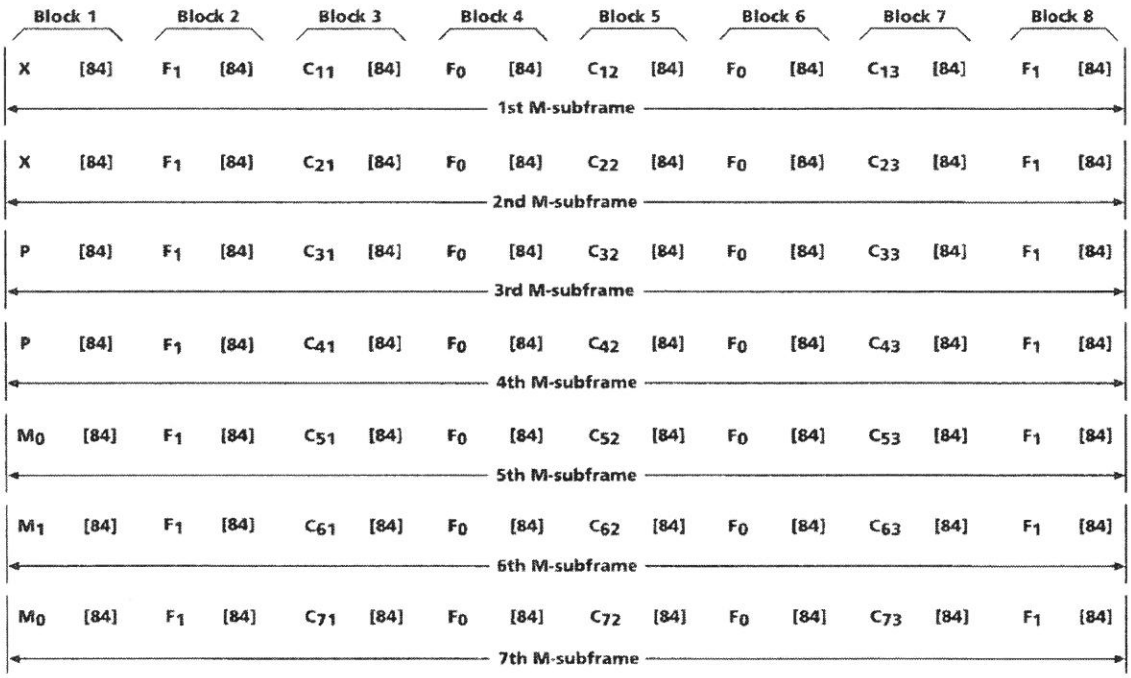
F-bits

The F-bits (framing bits) form the frame alignment signal. There are 28 F-bits per DS3 frame (four per subframe). The F-bits are located in the first bit position in blocks 2, 4, 6, and 8 of each subframe. The frame alignment pattern, which is repeated every subframe, is "1001".

The rate of framing bit errors is a good in-service approximation of the logic bit error rate because of the number and location of framing bits.

M-bits

The M-bits (multiframing bits) form the multiframe alignment signal. There are three M-bits per DS3 frame. The M-bits are located in the first bit position in block 1 of subframes 5, 6, and 7. DS3 equipment use the M-bit "010" pattern to locate the seven subframes.



NOTES:

1. $F_1 F_0 F_0 F_1$ is the frame alignment signal. $F_0 = 0$ and $F_1 = 1$
2. $M_0 M_1 M_0$ is the multiframe alignment signal. $M_0 = 0$ and $M_1 = 1$.
3. P is the parity information taken over all information bits in the preceding M-frame. Both P-bits equal 1 if the digital sum of all information bits is 1. Both P-bits equal 0 if the sum is 0.
4. The X-bits may be used for the transmission of in-service meassages. In any one M-frame the two X-bits must be identical and may not change more than once per second.
5. $C_{i1} C_{i2} C_{i3}$ = stuffing indicators for DS2 input i.
   $C_{21} C_{22} C_{23}$ = stuffing indicators for DS2 input 2.
   $C_{31} C_{32} C_{33}$ = stuffing indicators for DS2 input 3.
   $C_{41} C_{42} C_{43}$ = stuffing indicators for DS2 input 4.
   $C_{51} C_{52} C_{53}$ = stuffing indicators for DS2 input 5.
   $C_{61} C_{62} C_{63}$ = stuffing indicators for DS2 input 6.
   $C_{71} C_{72} C_{73}$ = stuffing indicators for DS2 input 7.
   If the three C-bits in subframe i are all zeros, no stuffing was done for DS2 input i. If the three C-bits are all ones, stuffing was done.
6. [84] represents 84 DS2 information bits between every DS3 OH bit.

Figure 4
DS3 overhead bits.

C-bits

The C-bits are used to control bit stuffing. There are three C-bits per subframe, designated C_{ij} (see ***Figure 4***), where i corresponds to the subframe number and j refers to the position number of the C-bit in a particular subframe. Refer to Appendix B on page 13 for details on how the C-bits are used to control bit stuffing within the DS3 frame.

X-bits

When a DS3 sink detects a condition for which framing cannot be found, or detects an alarm indication signal (AIS), it should declare a yellow alarm. If yellow alarm is implemented, the DS3 sink shall generate the alarm by setting the X-bits to zero (X1=0 and X2=0) in the returning DS3 signal. In the non-alarm condition, the X-bits shall be set to one (X1=1 a nd X2=1). The source shall not change the state of the X-bits more than once every second.

P-bits

The P-bits (parity bits) contain parity information. There are two P-bits per DS3 frame. The P-bits are located in the first bit position in block 1 of subframe 3 and subframe 4. DS3 sources compute parity over all 4,704 DS3 information bits (4,760 total bits – 56 OH bits) following the first X-bit in a DS3 frame. The resulting parity information is inserted in the P-bit positions of the following frame. The state of the two P-bits within a single DS3 frame is always identical. The two P-bits are set to "1" if the previous DS3 frame contained an odd number of ones. Conversely, the two P-bits are set to "0" if the previous DS3 frame contained an even number of ones.

The parity bits provide a means of in-service error detection. If, on the receive-side, the number of ones for a given frame does not match the parity information in the following frame, one or more bit errors occurred during the transmission.

C-bit Parity Framing Format

The standard M13 asynchronous format uses all 21 DS3 C-bits for bit stuffing control. Since M13 multiplexers perform bit stuffing when forming the seven DS2 signals from the 28 DS1 signals, the resulting DS2 signals are synchronous to each other. Therefore, the bit stuffing which takes place when the seven DS2 signals are multiplexed into the single DS3 signal is a redundant process.

By redefining the two-step multiplexing method, this redundant bit stuffing process can be eliminated. This redefinition results in a new format, called DS3 C-bit parity. The C-bit parity format, unlike the M13 format, does not use the DS3-level C-bits for bit stuffing control. Instead, the C-bits, as well as the X-bits, are redefined, making it possible to provide (a) in-service, end-to-end path performance monitoring of the DS3 signal, and (b) in-band data links.

C-bit Parity Format OH Bits

Figure 5 on the next page shows the OH bits within the C-bit parity format. The definitions for the framing, multiframing, and parity bits are the same as the definitions within the standard M13 asynchronous format. The new X-bit and C-bit definitions are described below (as per the T1X1.4 Working Group):

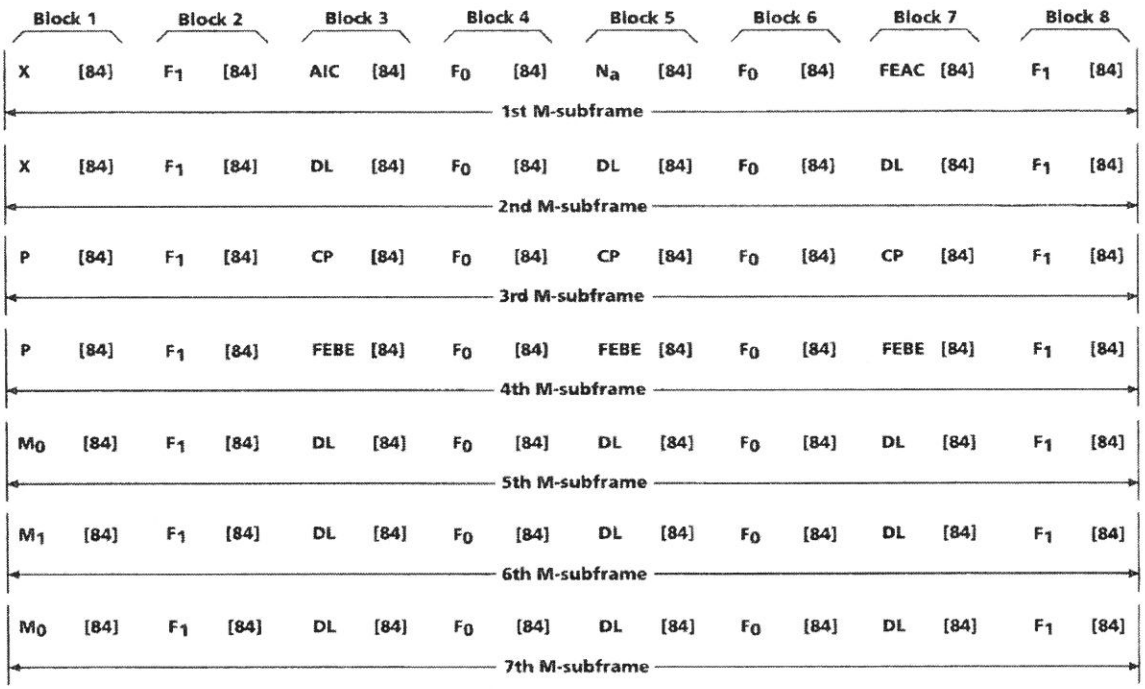
X-bits

In C-bit parity, the X-bit channel shall be used to transmit defects from the far end to the near end of the system in the same manner as remote alarm indicator (RAI). When a DS3 sink detects a severely errored frame (SEF-DS3 sink failed to frame on a received signal) or AIS defect, the associated DS3 source should be capable of controlling the setting of the X-bits. If this capability is implemented, the DS3 source shall set the X-bits to zero (X1=0 and X2=0) upon receipt of an SEF or AIS defect. The X-bits shall be set to one otherwise (X1=1 and X2=1). The DS3 source shall not change the state of the X-bits more than once every second.

C-bits

Application Identification Channel (AIC)

The first C-bit in subframe 1 is defined as an AIC and can be used by DS3 terminal equipment (TE) to automatically identify a specific DS3 framing format. For C-bit parity, this position is set to a "1".



NOTES:

1. $F_1F_0F_1$ is the frame alignment signal. $F_0 = 0$ and $F_1 = 1$.
2. $M_0M_1M_0$ is the multiframe alignment signal. $M_0 = 0$ and $M_1 = 1$.
3. P is the parity information taken over all information bits in the preceding M-frame. Both P-bits equal 1 if the digital sum of all information bits is 1. Both P-bits equal 0 if the sum is 0.
4. The X-bits are used to transmit a "degraded second" from the far-end to the near-end. In any one M-frame the two X-bits must be identical and may not change more than once per second.
5. C-bit definitions:
   - AIC = Application Identification Channel = 1.
   - N_a = Reserved Network Application Bit.
   - FEAC = Far-End Alarm and Control Channel.
   - DL = Data Link.
   - CP = C-bit Parity.
   - FEBE = Far-End Block Error.
6. [84] represents 84 DS2 information bits between every DS3 OH bit

Figure 5
C-bit parity overhead bits.

Reserved Network Application Bit

The second C-bit in subframe 1, designated N_a, is reserved for future applications.

Far-End Alarm and Control (FEAC) Channel

The third C-bit in subframe 1 is used as a FEAC channel, where alarm or status information from the far-end terminal can be sent back to the near-end terminal.

This channel is also used to initiate DS3 and DS1 line loopbacks at the far-end terminal from the near-end terminal. A simple, repeating, 16-bit code word, of the form

0XXXXXX011111111 where "X" can be a "0" or a "1"

with the rightmost bit transmitted first, can be used to indicate one of several possible alarm or status conditions. When no alarm or status condition is being transmitted, the FEAC channel is set to all ones. Refer to the latest document issued by the T1X1.4 Working Group for a complete listing of the FEAC code words.

Data Links (DL)

The 12 C-bits located in subframes 2, 5, 6, and 7, all designated DL, are defined as data links for applications and terminal-to-terminal path maintenance. Refer to the latest document issued by the T1X1.4 Working Group for a complete description of how these bits are used.

DS3 Path Parity Bits

The three C-bits in subframe 3, designated CP-bits, are used to carry the DS3 path parity information. At the DS3 TE transmitter the CP-bits are set to the same value as the two P-bits. Since the CP-bits will pass through the network unchanged (except in the case of errors), the DS3 TE receiver can determine if an error occured in an M-frame by computing the parity based on the contents of the given M-frame and comparing this parity value with the parity received in the CP-bits in the following M-frame.

NOTE: The normal P-bits cannot provide DS3 path monitoring because they are subject to correction by each facility section the the DS3 path. Therefore, the M13 format cannot provide end-to-end path parity information. The C-bit parity format has a big advantage over the M13 format by providing end-to-end parity checking.

Far-End Block Error (FEBE) Function

The FEBE function uses the three C-bits in subframe 4 and can best be understood as illustrated in the following example. Refer to ***Figure 6.*** The near-end TE monitors its incoming direction of transmission (west-bound) for the occurrence of a framing or parity error event. Upon detecting a framing or parity error event via the west-bound CP-bits, the near-end TE will (a) count the event as a C-bit parity error, and (b) indicate to the far-end TE the occurrence of the error via the east-bound FEBE bits by setting the three FEBE bits to "000" to indicate the error. (The three FEBE bits are set to "111" if no parity error event occurred.) Since DS3 TE monitors both the CP and FEBE bits, as well as the FEAC channel, the overall performance of the DS3 path, for both directions of transmission, can be determined at either end of the path.

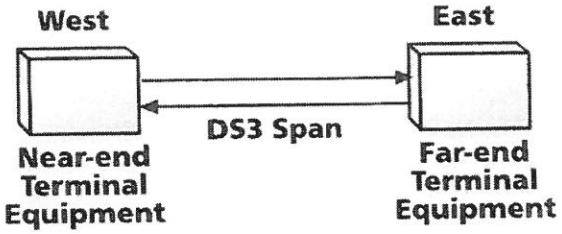


Figure 6
DS3 span.

Summary

The DS3 signal is composed of 28 DS1 signals and is constructed using a two-step multiplexing process. First, the 28 DS1 signals are multiplexed into seven DS2 signals. Second, the seven DS2 signals are multiplexed into one DS3 signal. Each multiplexing step uses bit stuffing to handle the different input frequencies. OH bits provide alignment, error checking, in-band communications, and bit stuffing control information.

The standard M13 format used widely today cannot provide end-to-end path parity information; a maintenance feature which is becoming more important as DS3 circuits become more prevalent. The C-bit parity format redefines the use of the C-bits in the M13 frame making it possible to provide in-service, end-to-end path performance monitoring of the DS3 signal and in-band data links. The ability to monitor degraded seconds, bidirectional end-to-end parity, and far-end alarms gives the C-bit parity format additional maintenance functionality over the M13 format.

Appendix A: The Mechanics of Bit Stuffing within the DS2 Frame

The DS2 C-bits are used as bit stuffing indicators during the first step of DS1-to-DS3 multiplexing: combining four DS1 signals into a single DS2 signal. There are three C-bits per DS2 subframe, designated C_{ij} (see ***Figure 2***), where i corresponds to the subframe number and j refers to the position number of the C-bit in a particular subframe.

In each DS2 frame one bit can be stuffed for each of the four DS1 signals. Specifically, the state of the three C-bits in the i^{th} subframe indicates whether or not bit stuffing occurs for the i^{th} DS1 input during the multiplexing process. The state of the C-bits is physically determined by the multiplexing equipment. If the three C-bits are all ones, stuffing occurs. The location if the stuffed bit is the first information bit position (designated 0_i) associated with the i^{th} DS1 signal following the last F_1 bit in a subframe. If the three C-bits are all zeros, no stuffing occurs and the associated "stuffable" bit position is merely treated as normal DS1 data bit.

During the demultiplexing process, the C-bits are used to determine if the "stuffable" bit is to be included in the reconstructed DS1 signal. For example, if $C_{21}=C_{22}=C_{23}=0$ then bit 0_2 following F_1 in the M2 subframe is a data bit and therefore is included in the reconstruction of the second DS1 signal. If $C_{21}=C_{22}=C_{23}=1$ then bit 0_2 following F_1 in the M2 subframe is a stuff bit and therefore is not included in the reconstruction of the second DS1 signal.

The purpose of using three C-bits instead of one is to minimize the chance of misidentifying the stuffing process if one of the C-bits is in error. Therefore, in actual practice, a majority vote of the three C-bits is used to more accurately control the stuffing process.

The ability to handle different DS1 signal rates can be calculated from the DS2 framing format. Since each DS2 frame allows for the stuffing of one bit for each of the four DS1 signals, the maximum stuffing rate for each DS1 signal is equal to the DS2 frame rate. A DS2 frame contains 1,176 bits as shown in ***Figure 1.*** Therefore the frame rate is:

6,312,000 bps ÷ 1,176 bits/frame =
5,367.35 frames/sec

and the number of OH bits per second is:

5,367.35 frames/sec x 24 OH bits/frame =
128,816.40 OH bps

The minimum stuffing rate is 0 bps. The actual bit stuffing rate depends on the rate of the DS1 signal. The bit stuffing rate for a DS1 signal operating at the nominal rate is calculated as follows:

Total DS2 bits	6,312,000 bps
Four DS1 signals (4 x 1.544 Mbps)	-6,176,000 bps
DS2 OH bits	-128,816 bps
Stuffing bits available	7,184 bps

These 7,184 bits are the total bits available for stuffing and are divided evenly over the four DS1 signals. Therefore, the bit stuffing rate for a DS1 signal operating at the nominal rate is:

7,184 bps ÷ 4 DS1 signals = 1,796 bps

The maximum allowable DS1 rate is computed as follows:

DS2 signal rate	6,312,000 bps
DS2 OH bits	-128,816 bps
Total DS1 bits	6,183,184 bps

The total number of DS1 bits is allocated evenly across the four DS1 signals:

6,183,184 bps ÷ 4 DS1 signals = 1,545,796 bps

Therefore each DS1 signal may be input at a maximum rate of 1,545,796 bps. The bit stuffing rate for a DS1 signal operating at this rate is 0 bps.

The minimum allowable DS1 rate is computed by taking the maximum allowable DS1 rate and subtracting the maximum stuffing rate (i.e., the DS2 frame rate) as follows:

Maximum DS1 rate	1,545,796 bps
Maximum stuff rate	-5,367 bps
Minimum DS1 rate	1,540,429 bps

Therefore each DS1 signal may be input at a minimum rate of 1,540,429 bps. The bit stuffing rate for a DS1 signal operating at this rate is 5,367 bps.

Figure 7 on the next page depicts a summary representation of the first step of DS1-to-DS3 M13-type multiplexing: combining four DS1 signals all operating at different rates. The DS1 input rates shown in ***Figure 7*** were chosen to demonstrate how the stuffing rates vary with different input rates. The DS2 output rate is the sum of all the following:

DS1 signal 1	1,544,000 bps (nom)
DS1 signal 1 stuff rate	1,796 bps
DS1 signal 2	1,545,796 bps (max)
DS1 signal 2 stuff rate	0 bps
DS1 signal 3	1,540,429 bps (min)
DS1 signal 3 stuff rate	5,367 bps
DS1 signal 4	1,544,500 bps (ex)
DS1 signal 4 stuff rate	1,296 bps
DS2 OH bits	128,816 bps
DS2 output rate	6,312,000 bps

NOTE:
1. The higher the DS1 rate the lower the associated bit stuffing rate because the sum of the two always totals to an "intermediate" DS1 rate of 1,545,796 bps.
2. The bit stuffing rate for a DS1 signal operating at the nominal rate of 1,544,000 bps is 1,796 bps.
3. The bit stuffing rate for a DS1 signal operating at the maximum rate of 1,545,796 bps is 0 bps.
4. The bit stuffing rate for a DS1 signal operating at the minimum rate of 1,540,429 bps is 5,367 bps.
5. The "intermediate" DS1 rate after bit stuffing is 1,545,796 bps (e.g., 1,544,000 bps + 1,796 bps) and is equal to the maximum DS1 input rate which can be tolerated.

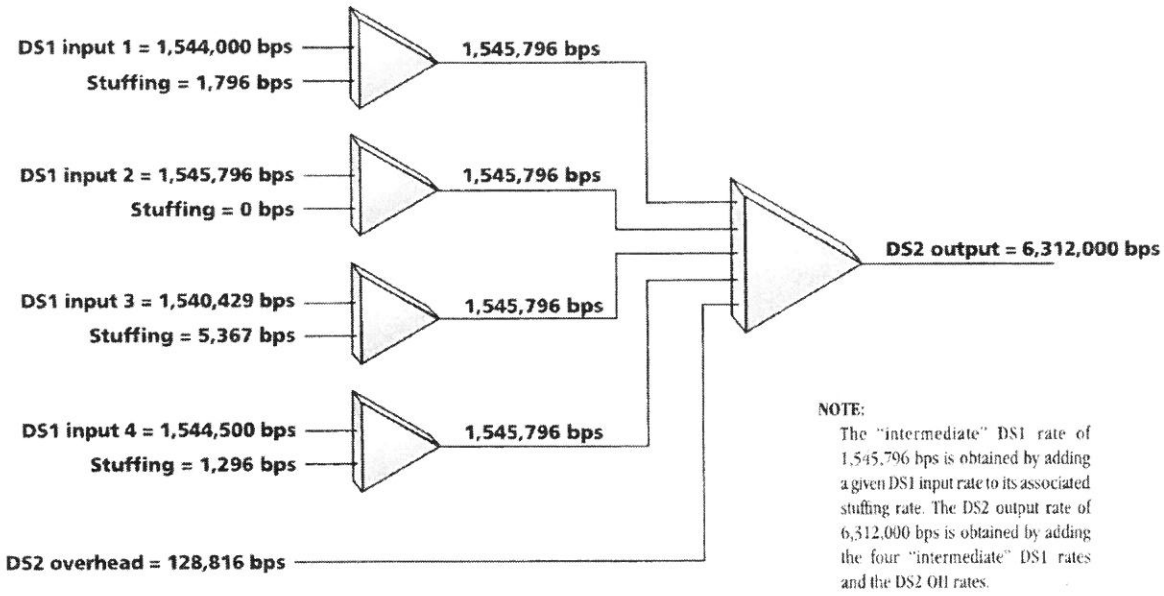


Figure 7
M13-type multiplexing of four DS1 signals.

Figure 8 shows how the minimum and maximum allowable DS1 rates fit into the typical operating mode of most DS1 communication systems. For M13-type multiplexing, the DS2 signal accepts DS1 input rates between 1,540,429 bps and 1,545,796 bps. This wide range of rates allows DS2 signals the flexibility to transmit proprietary encoded DS1 signals as well as the commonly used, framed 1,544,000 bps ±50 bps signal.

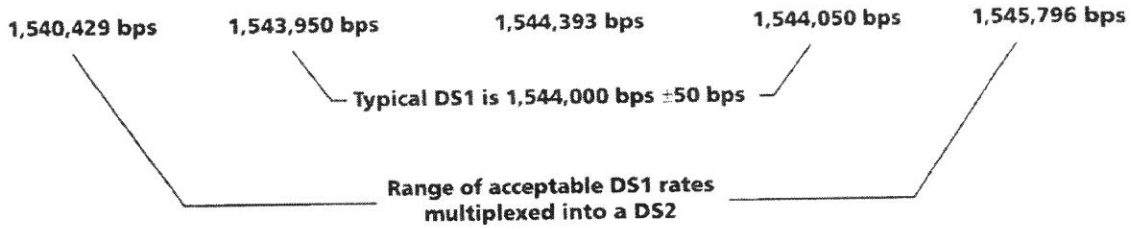


Figure 8
Range of DS1 rates.

Appendix B: The Mechanics of Bit Stuffing within the DS3 Frame

The DS3 C-bits are used as bit stuffing indicators during the second step of DS1-to-DS3 multiplexing: combining seven DS2 signals into a single DS3 signal. There are three C-bits per DS3 subframe, designated C_{ij} (see ***Figure 4***), where i corresponds to the subframe number and j refers to the position number of the C-bit in a particular subframe.

In each DS3 frame one bit can be stuffed for each of the seven DS2 signals. Specifically, the state of the three C-bits in the i^{th} subframe indicates whether or not bit stuffing occurs for the i^{th} DS2 input during the multiplexing process. The state of the C-bits is physically determined by the multiplexing equipment. If the three C-bits are all ones, stuffing occurs. The location of the stuffed bit is the first information bit position (designated 0_i) associated with the i^{th} DS2 signal following the last F_1 bit in a subframe. If the three C-bits are all zeros, no stuffing occurs and the associated "stuffable" bit position is merely treated as normal DS2 data bit.

During the demultiplexing process, the C-bits are used to determine if the "stuffable" bit is to be included in the reconstructed DS2 signal. For example, if $C_{61}=C_{62}=C_{63}=0$ then bit 0_6 following F_1 in the sixth M-subframe is a data bit and therefore is included in the reconstruction of the sixth DS2 signal. If $C_{61}=C_{62}=C_{63}=1$ then bit 0_6 following F_1 in the sixth M-subframe is a stuff bit and therefore is not included in the reconstruction of the sixth DS2 signal.

The purpose of using three C-bits instead of one is to minimize the chance of misidentifying the stuffing process if one of the C-bits is in error. Therefore, in actual practice, a majority vote of the three C-bits is used to more accurately control the stuffing process.

The ability to handle different DS2 signal rates can be calculated from the DS3 framing format. Since each DS3 frame allows for the stuffing of one bit for each

of the seven DS2 signals, the maximum stuffing rate for each DS2 signal is equal to the DS3 frame rate. A DS3 frame contains 4,760 bits as shown in ***Figure 3***. Therefore the frame rate is:

44,736,000 bps ÷ 4,760 bits/frame = 9,398.32 frames/sec

and the number of OH bits per second is:

9,398.32 frames/sec x 56 OH bits/frame = 526,305.92 OH bps

The minimum stuffing rate is 0 bps. The actual bit stuffing rate depends on the rate of the DS2 signal. The bit stuffing rate (for the M13 format) for a DS2 signal operating at the nominal rate is calculated as follows:

Total DS3 bits	44,736,000 bps
Seven DS2 signals (7 x 6.312 Mbps)	-44,184,000 bps
DS3 OH bits	-526,306 bps
Stuffing bits available	25,694 bps

These 25,694 bits are the total bits available for stuffing and are divided evenly over the seven DS2 signals. Therefore the bit stuffing rate for a DS2 signal operating at the nominal rate is:

25,694 bps ÷ 7 DS2 signals = 3,671 bps

The maximum allowable DS2 rate is computed as follows:

DS3 signal rate	44,736,000 bps
DS3 OH bits	-526,306 bps
Total DS2 bits	44,209,694 bps

The total number of DS2 bits is allocated evenly across the seven DS2 signals:

44,209,694 bps ÷ 7 DS2 signals = 6,315,671 bps

Therefore each DS2 signal may be input at a maximum rate of 6,315,671 bps. The bit stuffing rate (for the M13 format) for a DS2 signal operating at this rate is 0 bps.

The minimum allowable DS2 rate is computed by taking the maximum allowable DS2 rate and subtracting the maximum stuffing rate (i.e., the DS3 frame rate) as follows:

Maximum DS2 rate	6,315,671 bps
Maximum stuff rate	-9,398 bps
Minimum DS2 rate	6,306,272 bps

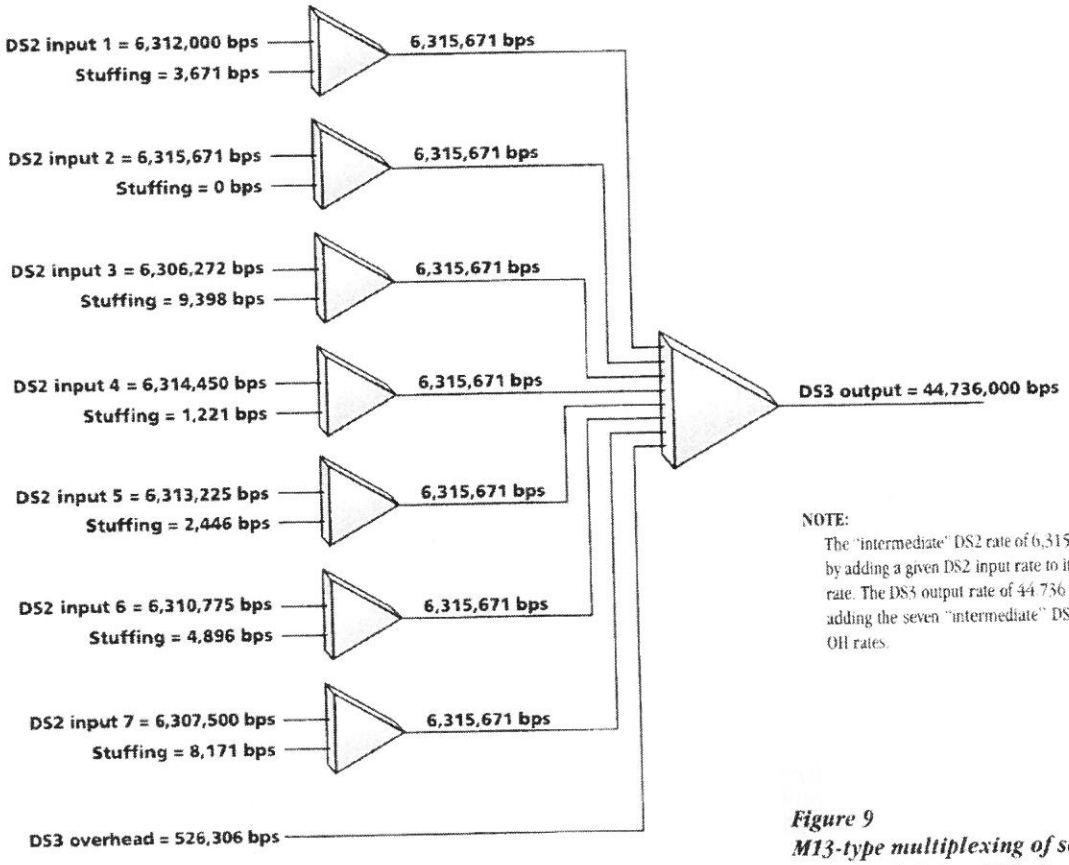
Therefore each DS2 signal may be input at a minimum rate of 6,306,272 bps. The bit stuffing rate (for the M13 format) for a DS2 signal operating at this rate is 9,398 bps.

Figure 9 depicts a summary representation of the second step of DS1-to-DS3 M13-type multiplexing: combining seven DS2 signals all operating at different rates. The DS2 input rates shown in ***Figure 9*** were chosen to demonstrate how the stuffing rates vary with different input rates. The DS3 output rate is the sum of all the following:

DS2 signal 1	6,312,000 bps (nom)
DS2 signal 1 stuff rate	3,671 bps
DS2 signal 2	6,315,671 bps (max)
DS2 signal 2 stuff rate	0 bps
DS2 signal 3	6,306,272 bps (min)
DS2 signal 3 stuff rate	9,398 bps
DS2 signal 4	6,314,450 bps (ex)
DS2 signal 4 stuff rate	1,221 bps
DS2 signal 5	6,313,225 bps (ex)
DS2 signal 5 stuff rate	2,446 bps
DS2 signal 6	6,310,775 bps (ex)
DS2 signal 6 stuff rate	4,896 bps
DS2 signal 7	6,307,500 bps (ex)
DS2 signal 7 stuff rate	8,171 bps
DS3 OH bits	526,306 bps
DS3 output rate	44,736,000 bps

NOTE:

1. The numbers do not add up exactly due to rounding off of the input frequencies.
2. The higher the DS2 rate the lower the associated bit stuffing rate because the sum of the two always totals to an "intermediate" DS2 rate of 6,315,671 bps.
3. The bit stuffing rate for a DS2 signal operating at the nominal rate of 6,312,000 bps is 3,671 bps.
4. The bit stuffing rate for a DS2 signal operating at the maximum rate of 6,315,671 bps is 0 bps.
5. The bit stuffing rate for a DS2 signal operating at the minimum rate of 6,306,272 bps is 9,398 bps.
6. The "intermediate" DS2 rate after bit stuffing is 6,315,671 bps (e.g., 6,312,000 bps + 3,671 bps) and is equal to the maximum DS2 input rate which can be tolerated.



NOTE:
The "intermediate" DS2 rate of 6,315,671 bps is obtained by adding a given DS2 input rate to its associated stuffing rate. The DS3 output rate of 44.736 Mbps is obtained by adding the seven "intermediate" DS2 rates and the DS3 OH rates.

Figure 9
M13-type multiplexing of seven DS2 signals into a DS3 signal.

Appendix C: Bit Stuffing for the C-bit Parity Format

The reader should have a good understanding of Appendices A and B before reading Appendix C.

DS1-to-DS3 multiplexing using the C-bit parity format is the same two-step multiplexing process defined for the standard M13 asynchronous format except that bit stuffing is done at every opportunity during the second step of multiplexing. Since stuffing occurs 100% of the time, the C-bits are no longer needed for bit stuffing control. However, this "full-time" bit stuffing at the DS3 level requires the seven DS2 signals to be lower in frequency than the 6.312 Mbps used with the standard M13 asynchronous format. Therefore, in the first step of multiplexing, four DS1 signals are multiplexed together to form a "pseudo" DS2 signal at a frequency of 6,306,272 bps. This frequency is chosen such that the seven "pseudo" DS2 signals are multiplexed, along with the "full-time" DS3-level stuff bits and the 56 OH bits, to give the nominal DS3 output frequency of 44.736 Mbps.

Figure 10 depicts a summary representation of the first step of DS1-to-DS3 C-bit parity-type multiplexing.

NOTE: The bit stuffing rates are lower than those used for the M13-type multiplexing (***Figure 7***) to yield an "intermediate" DS1 rate of 1,544,393 bps (instead of 1,545,796 bps) and hence a DS2 "pseudo" output rate of 6,306,272 bps (instead of 6,312,000 bps). This new "intermediate" DS1 rate forces the maximum allowable DS1 input rate (i.e., when bit stuffing is 0 bps) to be 1,544,393 bps.

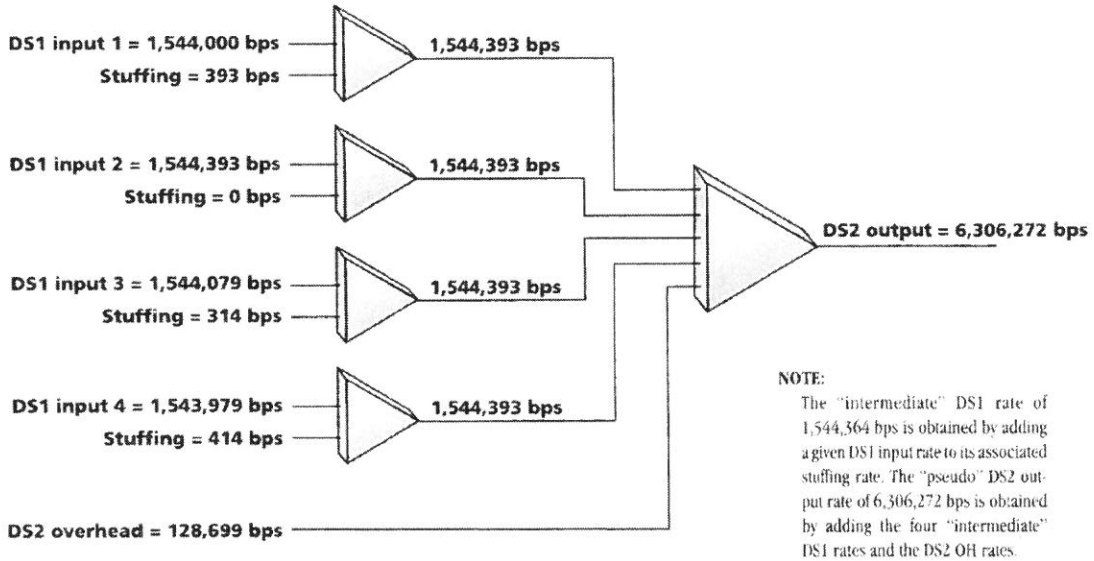


Figure 10
C-bit parity-type multiplexing of four DS1 signals.

If the multiplexing process shown in ***Figure 9*** were being done for the C-bit parity format instead of the standard M13 asynchronous format, the following would apply:

1. All the DS2 input rates would be at the "pseudo" frequency of 6,306,272 bps (instead of 6,312,000 bps).
2. All the stuffing rates would be at 9,398 bps, the maximum stuffing rate.
3. The "intermediate" DS2 rate after bit stuffing would still be 6,315,671 bps (6,306,272 bps + 9,398 bps).

Figure 11 shows the complete progression from a nominal DS1 rate (1.544 Mbps) to a nominal DS3 rate (44.736 Mbps) for both the standard M13 asynchronous format and the C-bit parity format.

	M13 Format	C-bit Format
Nominal DS1 rate	1,544,000 bps	1,544,000 bps
+ DS1 bit stuffing rate	1,796 bps	393 bps
= "intermediate" DS1 rate	1,545,796 bps	1,544,393 bps
x 4 DS1s per DS2	4	4
= subtotal	6,183,184 bps	6,177,572 bps
+ DS2 OH rate	128,816 bps	128,699 bps
= nominal DS2 rate	6,312,000 bps	6,306,272 bps
+ DS2 bit stuffing rate	3,671 bps	9,398 bps
= "intermediate" DS2 rate	6,315,671 bps	6,315,671 bps
x 7 DS2s per DS3	7	7
= subtotal	44,209,694 bps	44,209,694 bps
+ DS3 OH rate	526,306 bps	526,306 bps
= nominal DS3 rate	44,736,000 bps	44,736,000 bps

NOTE:
The calculations are not exact because each "intermediate" result is rounded off to the nearest whole number.

Figure 11
M13 format vs. C-bit format: progression from nominal DS1 to nominal DS3.

Appendix D: DS1, DS2, and DS3 Specification Summary

DS1

Line Rate:
1,544,000 bps

Channels:
24 8-bit DS0 channels/frame

OH Bits:
1 per frame

Total Bits:
193 bits/frame

DS2

Line Rate (M13 format):
6,312,000 bps

"Pseudo" Line Rate (C-bit parity format):
6,306,272 bps

Signals:
4 DS1 signals

OH Bits:
24 bits total/frame

F-bits (framing)	8 bits/frame
M-bits (multiframing)	4 bits/frame
C-bits (stuffing)	12 bits/frame
Data bits between OH bits	48

OH Bit Sequence:
M_0 [48] C_{11} [48] F_0 [48] C_{12} [48] C_{13} [48] F_1
M_1 [48] C_{21} [48] F_0 [48] C_{22} [48] C_{23} [48] F_1
M_1 [48] C_{31} [48] F_0 [48] C_{32} [48] C_{33} [48] F_1
M_x [48] C_{31} [48] F_0 [48] C_{42} [48] C_{43} [48] F_1

Total Bits:
1,176 bits/frame

Total DS1 Information Bits:
1,152 bits/frame

Frame:
4 subframes

Subframe:
6 blocks

Block:
49 bits (48 data bits and 1 OH bit)

Frame Alignment Pattern (F-bits):
"01" every subframe

Multiframe Alignment Pattern (M-bits):
"011X" every frame

OH Bit Rate:
128,816 b/s (M13 format)

Stuffing Rates per DS1:
Maximum:
5,367 bps (DS1 min. rate = 1,540,429 bps)
Nominal (M13 format):
1,796 bps (DS1 nom. rate = 1,544,000 bps)
Nominal (C-bit format):
393 bps (DS1 nom. rate = 1,544,000 bps)
Minimum:
0 bps (DS1 max. rate = 1,545,796 bps)

DS3

Line Rate:
44,736,000 bps

Signals:
7 DS2 signals = 28 DS1 signals

OH Bits:
56 bits total/frame

F-bits (framing)	28 bits/frame
M-bits (multiframing)	3 bits/frame
C-bits (stuffing)	21 bits/frame
X-bits (message)	2 bits/frame
P-bits (parity)	2 bits/frame
Data bits between OH bits	84

OH Bit Sequence:

X [84] F_1 [84] C_{11} [84] F_0 [84] C_{12} [84] F_0 [84] C_{13} [84] F_1
X [84] F_1 [84] C_{21} [84] F_0 [84] C_{22} [84] F_0 [84] C_{23} [84] F_1
P [84] F_1 [84] C_{31} [84] F_0 [84] C_{32} [84] F_0 [84] C_{33} [84] F_1
P [84] F_1 [84] C_{41} [84] F_0 [84] C_{42} [84] F_0 [84] C_{43} [84] F_1
M_0 [84] F_1 [84] C_{51} [84] F_0 [84] C_{52} [84] F_0 [84] C_{53} [84] F_1
M_1 [84] F_1 [84] C_{61} [84] F_0 [84] C_{62} [84] F_0 [84] C_{63} [84] F_1
M_0 [84] F_1 [84] C_{71} [84] F_0 [84] C_{72} [84] F_0 [84] C_{73} [84] F_1

Total Bits:
4,760 bits/frame

Total DS2 Information Bits:
4,704 bits/frame

Frame:
7 subframes

Subframe:
8 blocks

Block:
85 bits (84 data bits and 1 OH bit)

Frame Alignment Pattern (F-bits):
"1001" every subframe

Multiframe Alignment Pattern (M-bits):
"010" every frame

OH Bit Rate:
526,306 bps

Stuffing Rates per DS2:
Maximum[1]:
9,398 bps (DS2 min. rate = 6,306,272 bps)
Nominal:
3,671 bps (DS2 nom. rate = 6,312,000 bps)
Minimum:
0 bps (DS2 max. rate = 6,315,671 bps)

[1]Stuffing is always set for the maximum rate for the C-bit parity format